Ordering number:ENN1334D

PNP/NPN Epitaxial Planar Silicon Transistors

2SA1319/2SC3332

High-Voltage Switching Applications

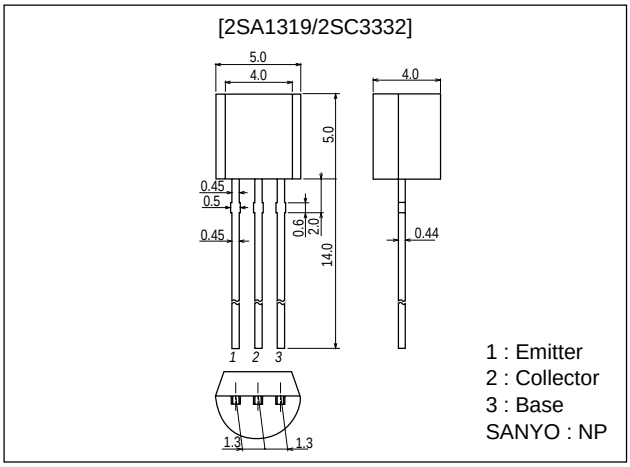
Features

- Hgih breakdown voltage.
- Excellent h_{FE} linearity.
- Wide ASO and highly resistant to breakdown.
- Adoption of MBIT process.

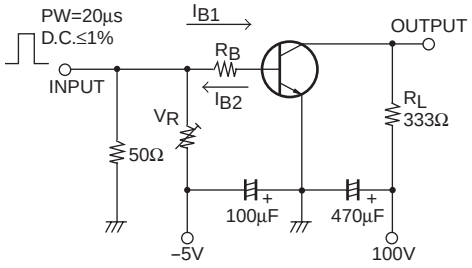
Package Dimensions

unit:mm

2003B



Switching Test Circuit



$20I_{B1}=-20I_{B2}=I_C=300mA$

(For PNP, the polarity is reversed.)

( ) : 2SA1319

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		(–)180	V
Collector-to-Emitter Voltage	V_{CEO}		(–)160	V
Emitter-to-Base Voltage	V_{EBO}		(–)6	V
Collector Current	I_C		(–)0.7	A
Collector Current (Pulse)	I_{CP}		(–)1.5	A
Collector Dissipation	P_C		700	mW
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=(–)120V, I_E=0			(–)0.1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(–)4V, I_C=0			(–)0.1	μA
DC Current Gain	$h_{FE}1$	V_{CE}=(–)5V, I_C=(–)100mA	100*		400*	
	$h_{FE}2$	V_{CE}=(–)5V, I_C=(–)10mA	80			

* : The 2SA1319/2SC3332 are classified by 100mA h_{FE} as follows :

Continued on next page.

Rank	R	S	T
h_{FE}	100 to 200	140 to 280	200 to 400

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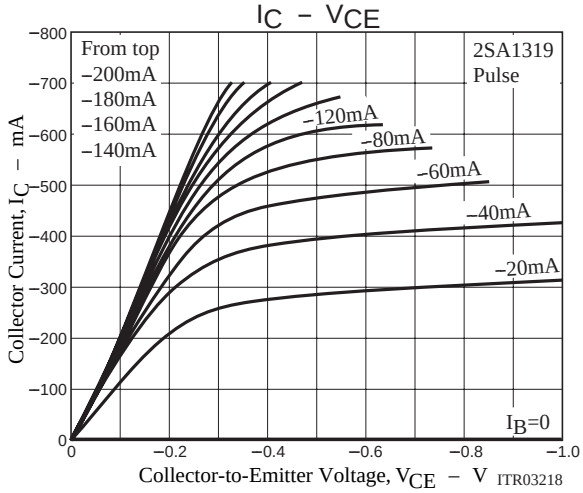
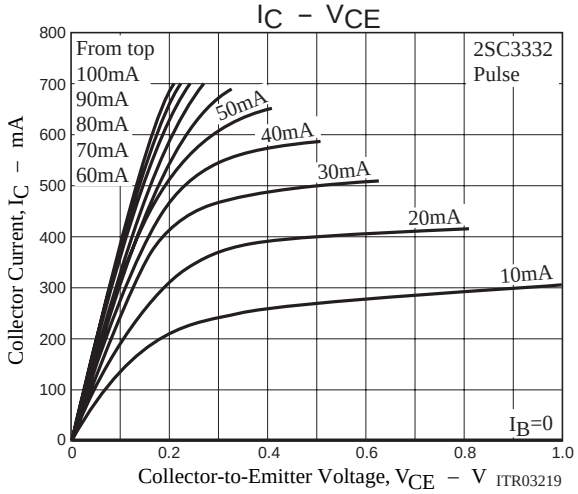
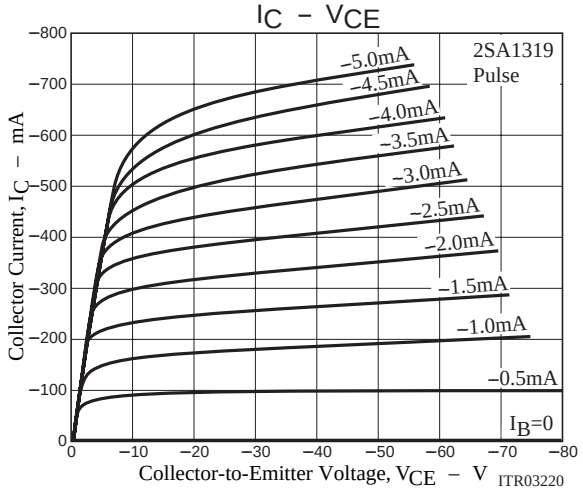
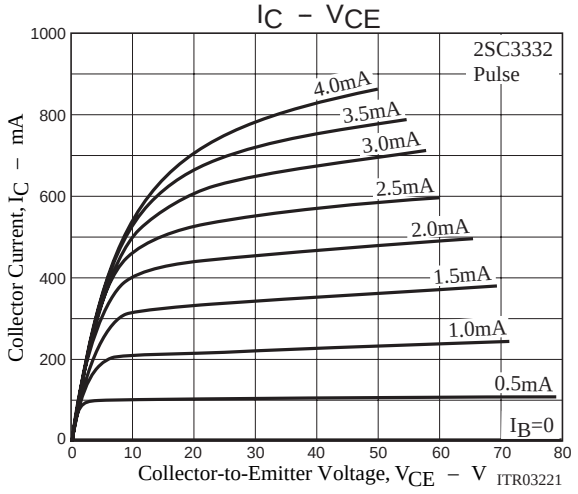
Continued from preceding page.

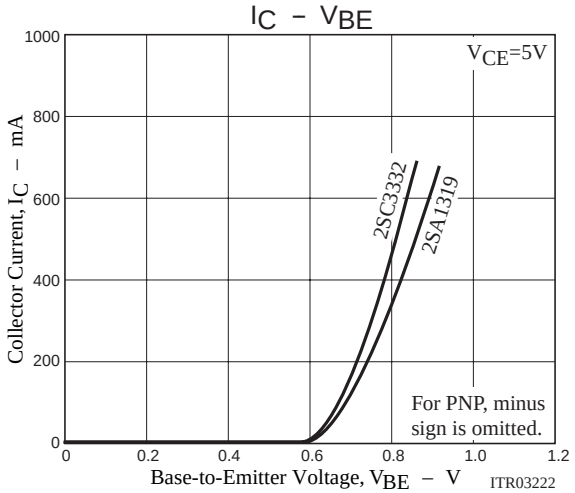
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gain Bandwidth Product	f_T	V_{CE}=(–)10V, I_C=(–)50mA		120		MHz
Common Base Output Capacitance	C_{ob}	V_{CB}=(–)10V		(11)8		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=(–)250mA, I_B=(–)25mA		(0.20) 0.12	(0.5) 0.4	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=(–)250mA, I_B=(–)25mA		(–)0.85	(–)1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=(–)10μA, I_E=0	(–)180			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=(–)1mA, R_{BE}=∞	(–)160			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=(–)10μA, I_C=0	(–)6			V
Turn-ON Time	t_{on}	See specified Test Circuit		(60)50		ns
Storage Time	t_{stg}	See specified Test Circuit		(900) 1000		ns
Fall Time	t_f	See specified Test Circuit		(60)60		ns

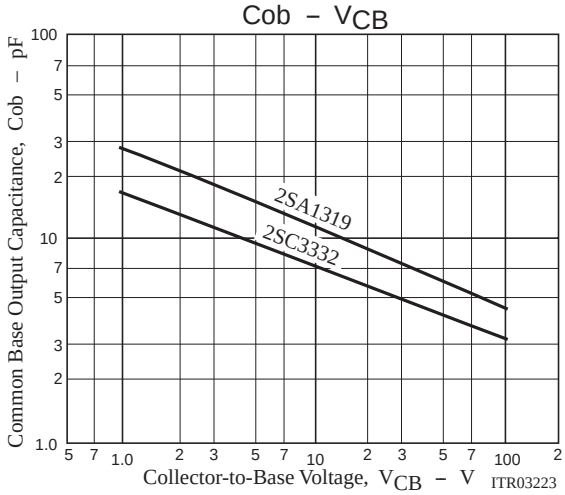




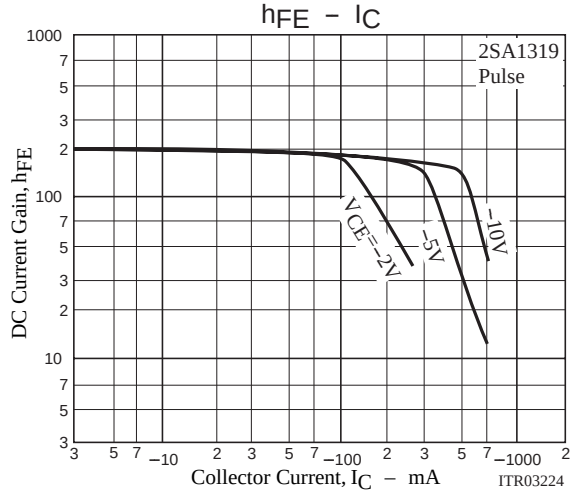




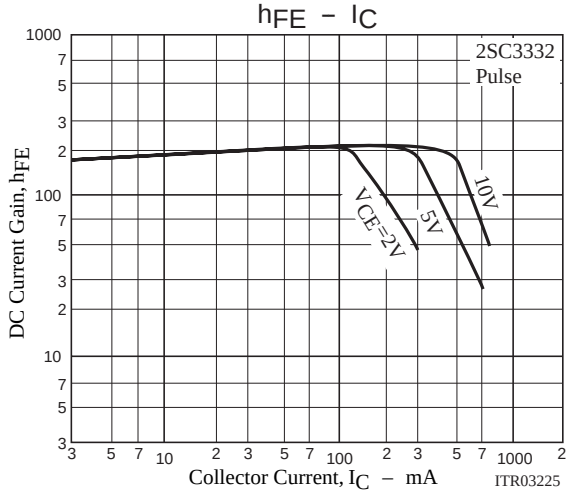




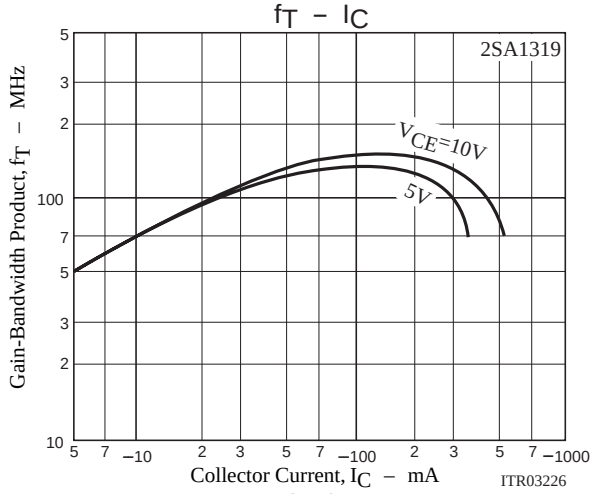
h_{FE} – I_C



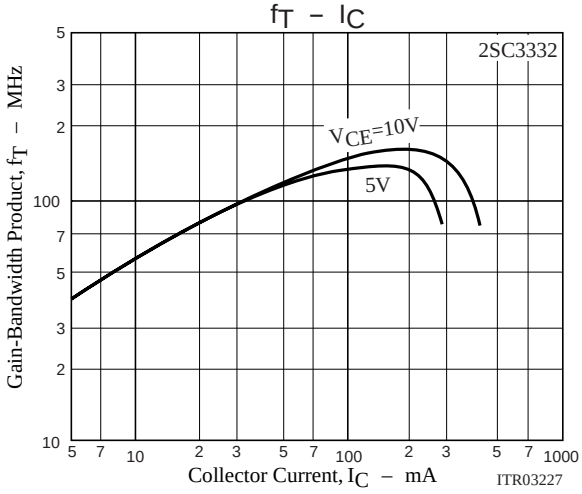
h_{FE} – I_C



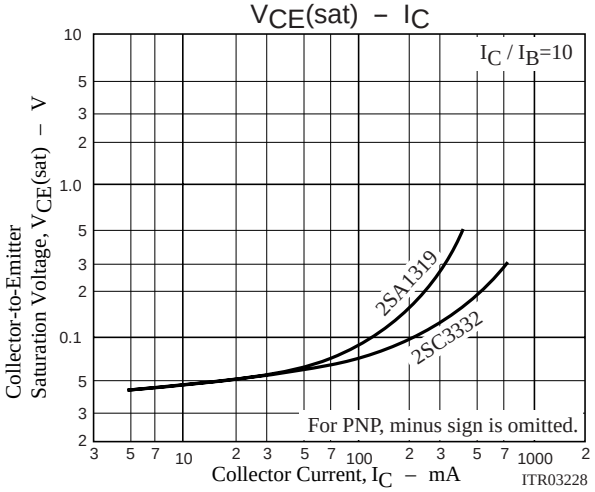
f_T – I_C



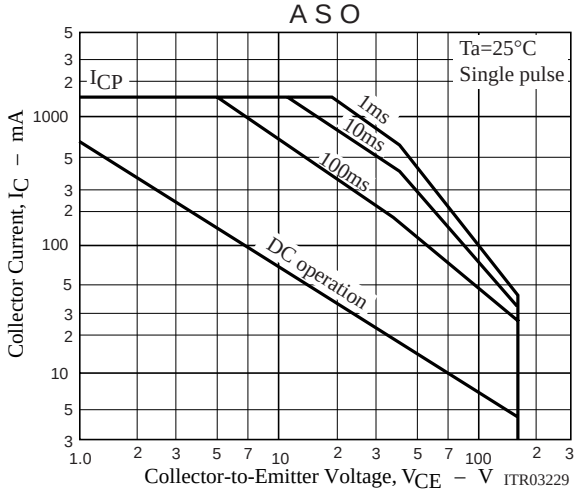
f_T – I_C



$V_{CE}(sat)$ – I_C



A S O



P_C – Ta