

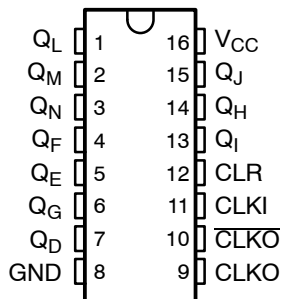
# SN74HC4060-Q1

## 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

SCLS726 – DECEMBER 2011

- Qualified for Automotive Applications
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Allow Design of Either RC- or Crystal-Oscillator Circuits

SN74HC4060-Q1 . . . D PACKAGE  
(TOP VIEW)



### description/ordering information

The 'HC4060-Q1 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock (CLKI) input increments the counter. A high level at the clear (CLR) input disables the oscillator ( $\overline{\text{CLKO}}$  goes high and CLKO goes low) and resets the counter to zero (all Q outputs low).

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - D    Reel of 2500	SN74HC4060QDRQ1	HC4060Q

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74HC4060-Q1

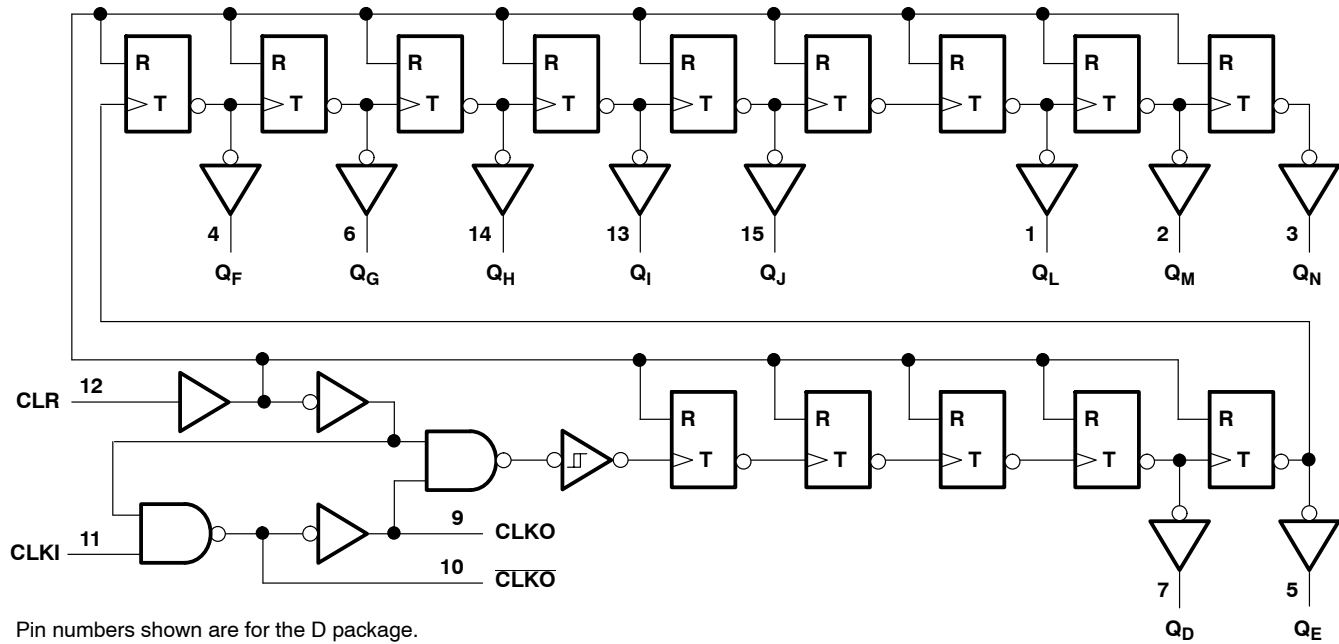
## 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

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FUNCTION TABLE  
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

### Logic diagram (positive logic)



Pin numbers shown are for the D package.

### Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C
ESD rating: Human Body Model (HBM)	2000 V
Charged Device Model (CDM)	1000 V
Machine Model (MM)	200 V

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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### Recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		V
		V <sub>CC</sub> = 4.5 V	1.35		
		V <sub>CC</sub> = 6 V	1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V	1000		ns
		V <sub>CC</sub> = 4.5 V	500		
		V <sub>CC</sub> = 6 V	400		
T <sub>A</sub>	Operating free-air temperature	-40	125		°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			'HC4060-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	All outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ,	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9		V	
				4.5 V	4.4	4.499	4.4			
				6 V	5.9	5.999	5.9			
	Q outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7			
I <sub>OH</sub> = -5.2 mA			6 V	5.48	5.8	5.2				
V <sub>OL</sub>	All outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ,	I <sub>OL</sub> = 20 μA	2 V	0.002		0.1	0.1	V	
				4.5 V	0.001		0.1	0.1		
				6 V	0.001		0.1	0.1		
	Q outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 4 mA	4.5 V	0.17		0.26	0.4		
I <sub>OL</sub> = 5.2 mA			6 V	0.15		0.26	0.4			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0			6 V	±0.1	±100	±1000		nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0,		I <sub>O</sub> = 0	6 V			8	160	μA	
C <sub>i</sub>				2 V to 6 V	3		10	10	pF	



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## 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

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Timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		'HC4060-Q1		UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	5.5		3.7		MHz
		4.5 V	28		19		
		6 V	33		22		
t <sub>w</sub>	CLKI high or low	2 V	90		135		ns
		4.5 V	18		27		
		6 V	15		23		
	CLR high	2 V	90		135		
		4.5 V	18		27		
		6 V	15		23		
t <sub>su</sub>	Setup time, CLR inactive before CLKI↓	2 V	160		240		ns
		4.5 V	32		48		
		6 V	27		41		

Switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

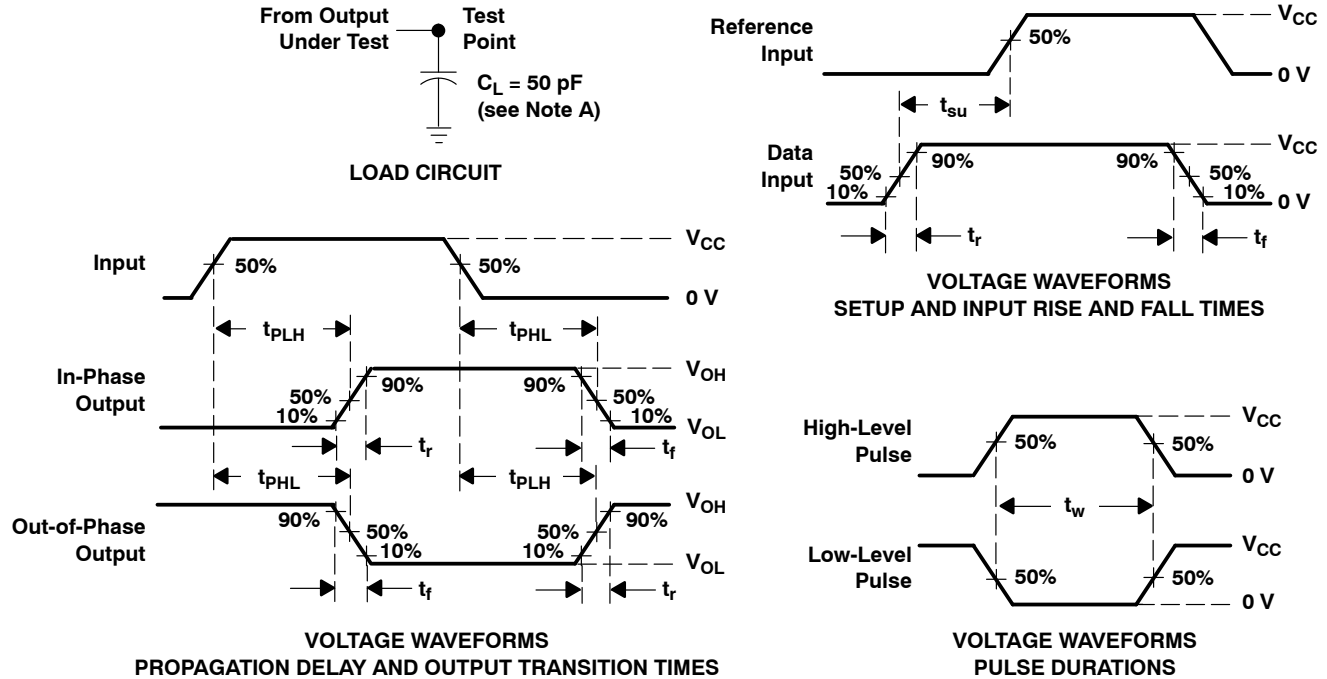
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			'HC4060-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			2 V	5.5	10		3.7		MHz
			4.5 V	28	45		19		
			6 V	33	53		22		
t <sub>pd</sub>	CLKI	Q <sub>D</sub>	2 V		240	490	735		ns
			4.5 V		58	98	147		
			6 V		42	83	125		
t <sub>PHL</sub>	CLR	Any Q	2 V		66	140	210		ns
			4.5 V		18	28	42		
			6 V		14	24	36		
t <sub>t</sub>		Any	2 V		28	75	110		ns
			4.5 V		8	15	22		
			6 V		6	30	19		

Operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	88	pF



### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

# SN74HC4060-Q1

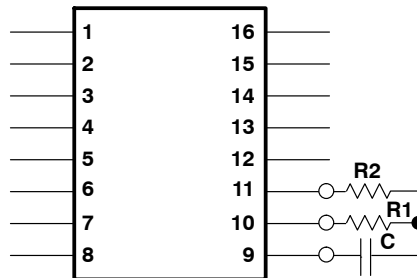
## 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

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### CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE 'HC4060-Q1 DEVICE

The 'HC4060-Q1 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405 R2}{R1 + R2} + 0.693\right)}$$

If  $R2 \gg R1$  (i.e.,  $R2 = 10R1$ ), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74HC4060QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### OTHER QUALIFIED VERSIONS OF SN74HC4060-Q1 :

● Catalog: [SN74HC4060](#)

● Military: [SN54HC4060](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4060QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4060QDRQ1	SOIC	D	16	2500	367.0	367.0	38.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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