

AN6346N

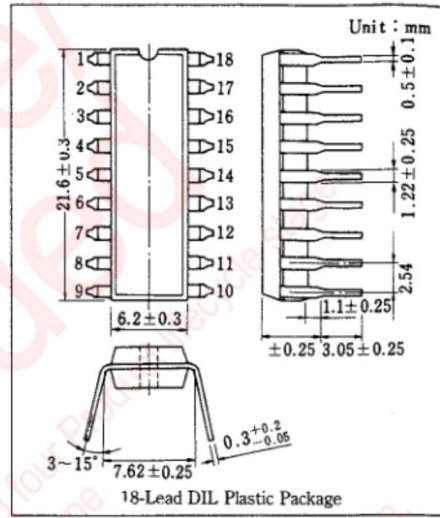
VTR Cylinder Interface Circuit

Outline

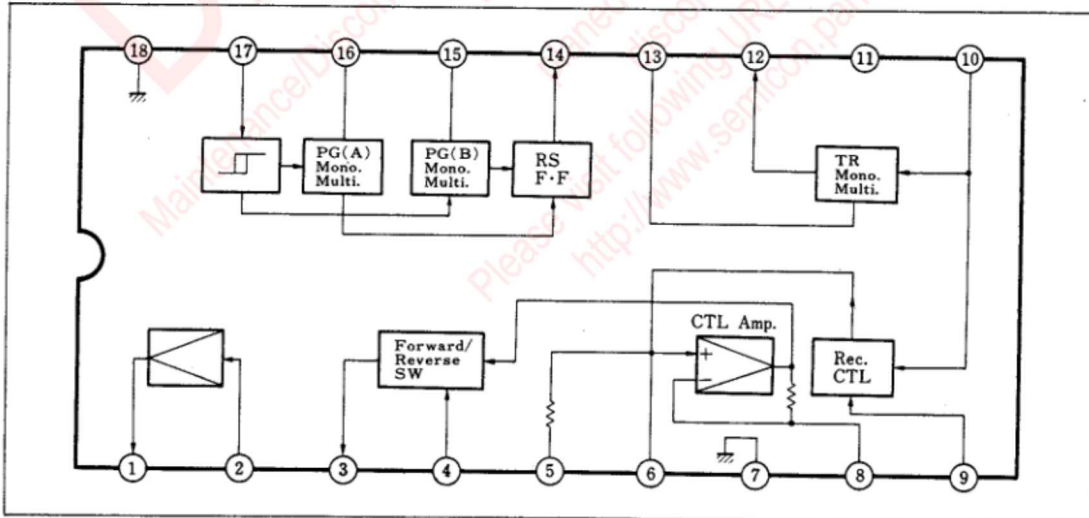
The AN6346N is an integrated circuit designed for VTR cylinder interface.

Features

- The functions consist of:
 - PG monostable multivibrator
 - Tracking monostable multivibrator
 - CTL amplifier
- Supply voltage: 5V



Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	P.B. CTL Output	10	1/2 V _{SS} Input
2	P.B. CTL Clamp Input	11	V _{CC}
3	P.B. CTL Amp. Output	12	Tracking Mono. Multi. Output
4	Forward/Reverse Select	13	Tracking Mono. Multi. Control
5	1/2 V _{CC}	14	Head Switch Output
6	CTL Signal	15	PG (B) Mono. Multi.
		16	PG (A) Mono. Multi.
7	GND	17	Cylinder PG Input
8	CTL Amp. Feedback	18	GND
9	Rec./P.B. Select	—	—

■ Absolute Maximum Ratings (T_a=25°C)

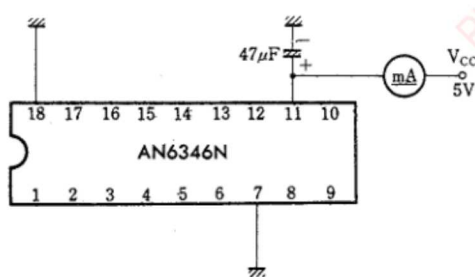
Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	6	V
Power dissipation (T _a =70°C)	P _D	100	mW
Operating ambient temperature	T _{opr}	-20 ~ +70	°C
Storage temperature	T _{stg}	-40 ~ +150	°C

■ Electrical Characteristics (V_{CC}=5 V, T_a=25°C ± 2°C)

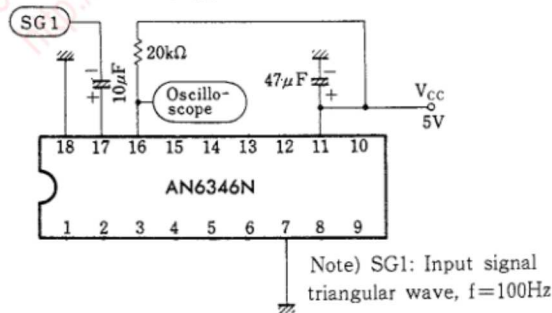
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current	I _{I1}	1	Without load	7.0		14	mA
PG amp. input sensitivity	S ₁₇	2		±65			mV
PG A mono. multi. delay amount	T ₁₆	3	C=0.056 μF, R=20kΩ	690		860	μs
PG B mono. multi. delay amount	T ₁₅	3	C=0.056 μF, R=20kΩ	690		860	μs
H/SW high-level output	V _{OH14}	4	Without load	4.6			V
H/SW low-level input	V _{OL14}	4	Without load			0.4	V
1/2 V _{SS} input sensitivity	S ₁₀	5				1.5	V
Rec. start select sensitivity	S ₉	6		3.0			V
For/Rev. select sensitivity	S ₄	7		3.0			V
Rec. CTL high-level output	V _{OH6}	8	Without load	4.0			V
Rec. CTL low-level output	V _{OL6}	8	Without load			0.4	V
P.B. CTL amp. gain (For.)	G _{FB3}	9	Without load	60		72	dB
P.B. CTL amp. gain (Rev.)	G _{RB3}	9		59		72	dB
Tracking mono. multi. delay amount	T ₁₃	10	C=0.27 μF, R=100kΩ	18		22	ms
P.B. CTL wave shaping input sensitivity	S ₂	11		300			mV

Note) Operating supply voltage range V_{CC(oper)}4.5~5.5V

Test Circuit 1 (I_{I1})

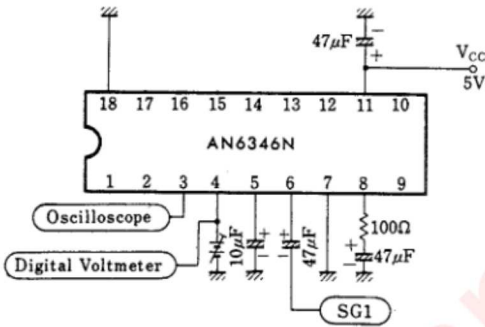


Test Circuit 2 (S₁₇)



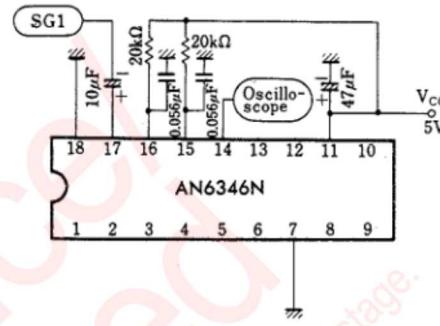
Note) SG1: Input signal triangular wave, f=100Hz

Test Circuit 3 (T_{16} , T_{15})



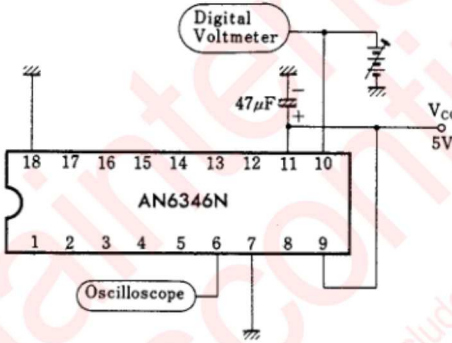
Note) SG1: Input signal sine wave $f=1\text{kHz}$, 0.2mVp-p

Test Circuit 4 (V_{OH14} , V_{OL14})



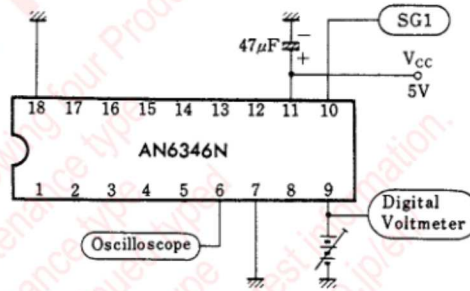
Note) SG1: Input signal triangular wave, $f=100\text{Hz}$, 1Vp-p

Test Circuit 5 (S_{10})



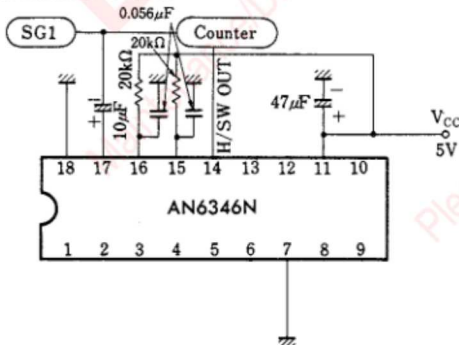
Note) Measure the Pin⑩ voltage at which Pin⑥ output changes after IC internal R-S FF setting (applying pulses to the Pin⑩ in the circuit above).

Test Circuit 6 (S_9)



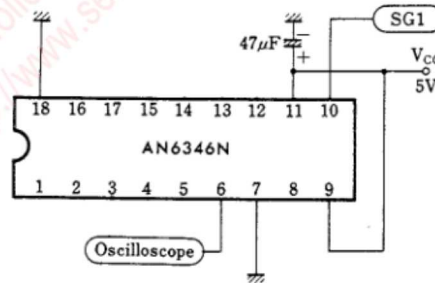
Note) SG1: Input signal rectangular wave, $f=30\text{Hz}$, 5Vo-p . Measure the Pin⑨ voltage at which no output is made to the Pin⑥.

Test Circuit 7 (S_4)



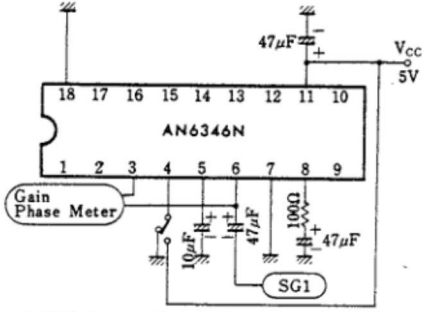
Note) SG1: Input signal rectangular wave, $f=100\text{Hz}$, 1Vp-p . T_{15} is a time from a fall of SG1 input signal to a rise of H/SW.OUT. T_{16} is a time from a rise of SG1 input signal to a fall of H/SW.OUT.

Test Circuit 8 (V_{OH6} , V_{OL6})



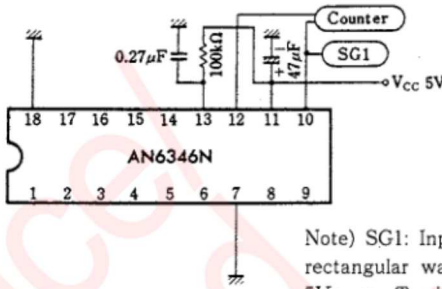
Note) SG1: Input signal rectangular wave, $f=30\text{Hz}$, 5Vo-p

Test Circuit 9 (G_{F3} , G_{R3})



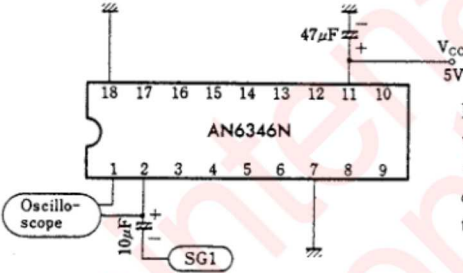
Note) SG1: Input signal sine wave, $f=1\text{kHz}$, $0.2\text{mV}_{\text{p-p}}$. G_{F3} for Pin④ GND, G_{R3} for Pin④ V_{CC}

Test Circuit 10 (T_{13})



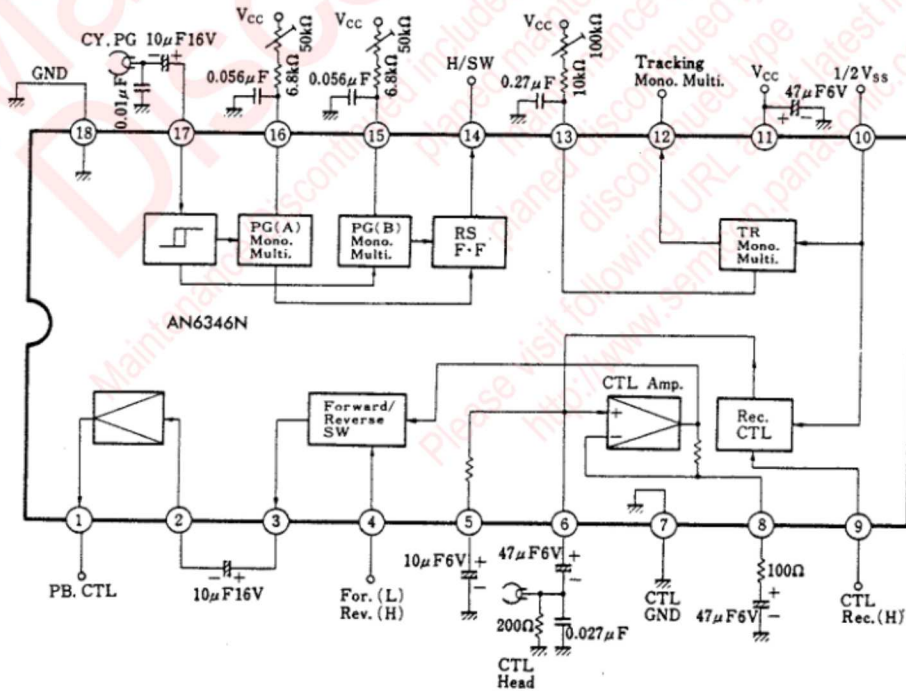
Note) SG1: Input signal rectangular wave, $f=30\text{Hz}$, $5\text{V}_{\text{O-p}}$. T_{13} is a time from a rise of SG1 to a fall of Pin② output.

Test Circuit 11 (S_2)



Note) SG1: Input signal rectangular wave, $f=30\text{Hz}$. $V_{\text{H}}-V_{\text{L}}$ of SG1 = S_2 when an SG1 signal level is changed and a signal is issued to the Pin①

Application Circuit



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