ALPHA & OMEGA SEMICONDUCTOR

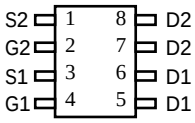
AO4601
Complementary Enhancement Mode Field Effect Transistor

General Description

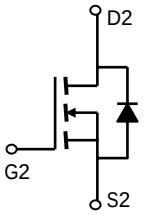
The AO4601 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. *Standard Product AO4601 is Pb-free (meets ROHS & Sony 259 specifications). AO4601L is a Green Product ordering option. AO4601 and AO4601L are*

Features

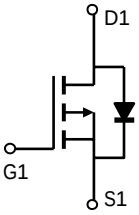
n-channel	p-channel
V_{DS} (V) = 30V	-30V
I_D = 4.7A (V_{GS}=10V)	-8A (V_{GS} = -20V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 55mΩ (V_{GS}=10V)	< 18mΩ (V_{GS} = -20V)
< 70mΩ (V_{GS}=4.5V)	< 19mΩ (V_{GS} = -10V)
< 110mΩ (V_{GS} = 2.5V)	



SOIC-8



n-channel



p-channel

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±12	±25	V
Continuous Drain Current [A]	T_A=25°C	I_D	4.7	-8	A
	T_A=70°C		4	-6.9	
Pulsed Drain Current [B]		I_{DM}	30	-50	
Power Dissipation	T_A=25°C	P_D	2	2	W
	T_A=70°C		1.44	1.44	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	-55 to 150	°C

Thermal Characteristics: n-channel and p-channel

Parameter		Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	n-ch	52	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		n-ch	78	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	n-ch	48	60	°C/W
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	p-ch	50	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		p-ch	73	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	p-ch	31	40	°C/W

n-channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	0.6	1	1.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	10			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=4A		45	55	mΩ
		T_J=125°C		66	80	
		V_{GS}=4.5V, I_D=3A		55	70	mΩ
		V_{GS}=2.5V, I_D=2A		83	110	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=4A		8		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.8	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		390		pF
C_{oss}	Output Capacitance			54.5		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		3		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=4A		0.6		nC
Q_{gs}	Gate Source Charge			1.38		nC
Q_{gd}	Gate Drain Charge			4.34		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=3.75Ω, R_{GEN}=6Ω		3.3		ns
t_r	Turn-On Rise Time			1		ns
$t_{D(off)}$	Turn-Off DelayTime			21.7		ns
t_f	Turn-Off Fall Time			2.1		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=4A, dI/dt=100A/µs		12		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=4A, dI/dt=100A/µs		6.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80 µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev 3 : Sept 2005

N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

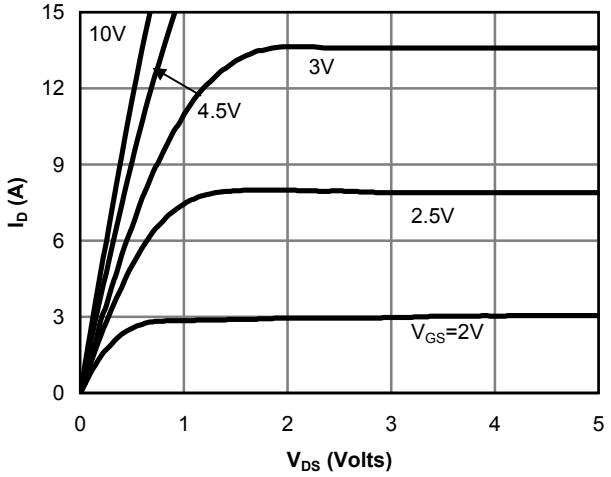


Fig 1: On-Region Characteristics

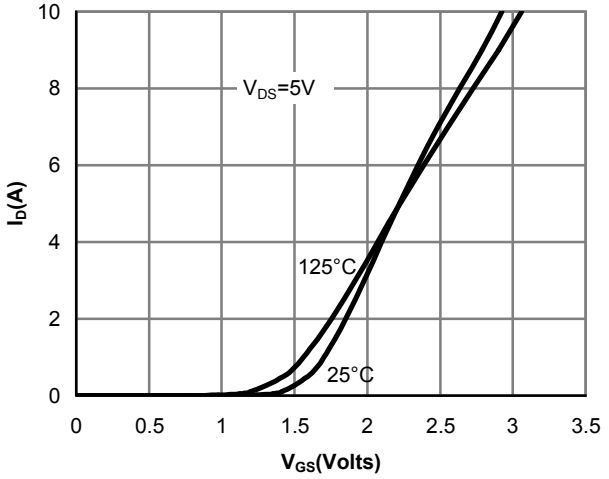


Figure 2: Transfer Characteristics

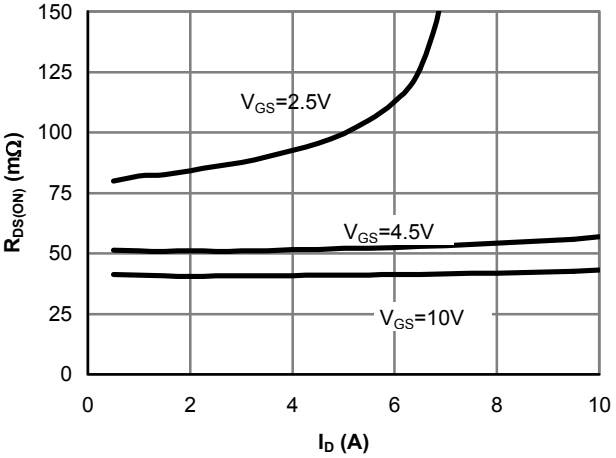


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

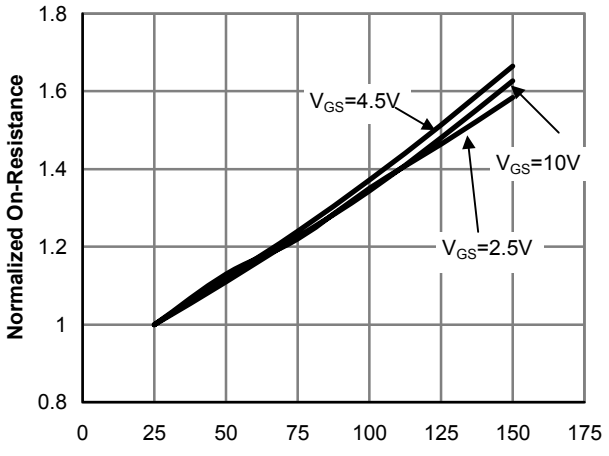


Figure 4: On-Resistance vs. Junction Temperature

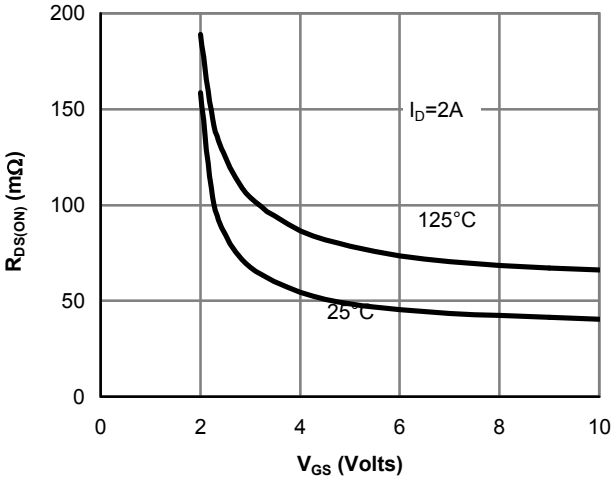


Figure 5: On-Resistance vs. Gate-Source Voltage

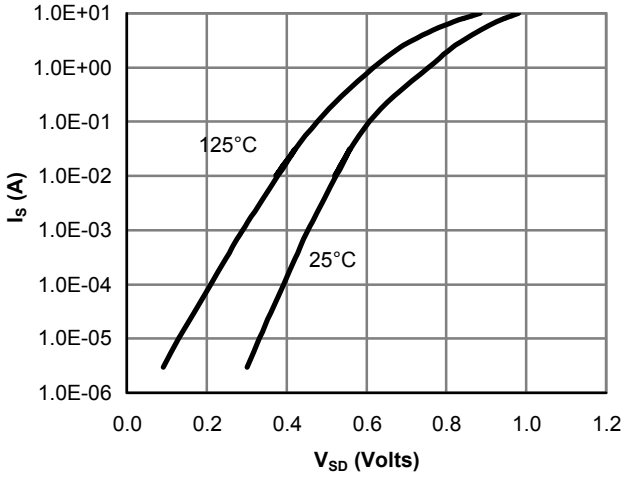


Figure 6: Body-Diode Characteristics

N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

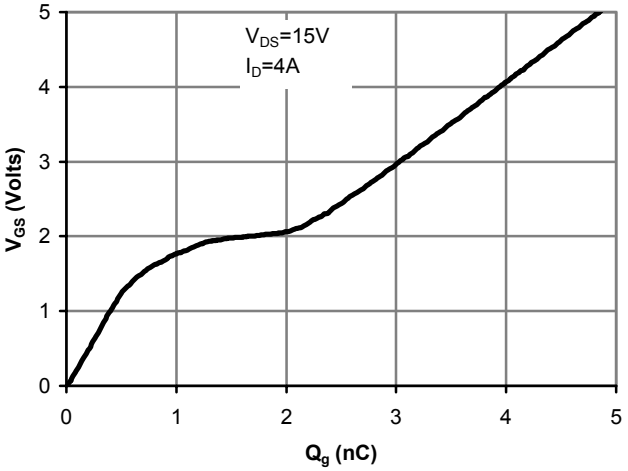


Figure 7: Gate-Charge Characteristics

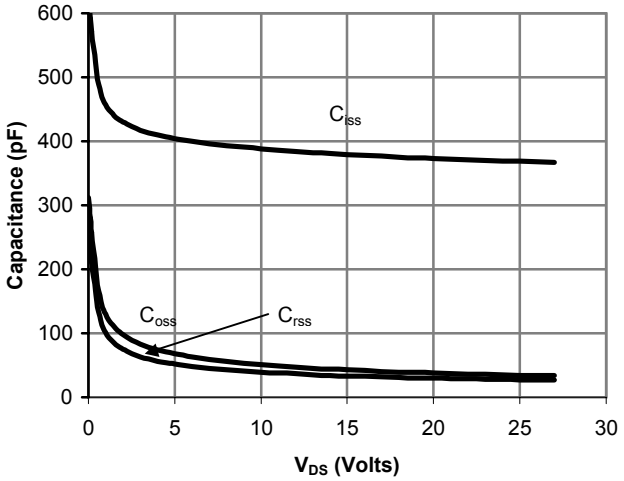


Figure 8: Capacitance Characteristics

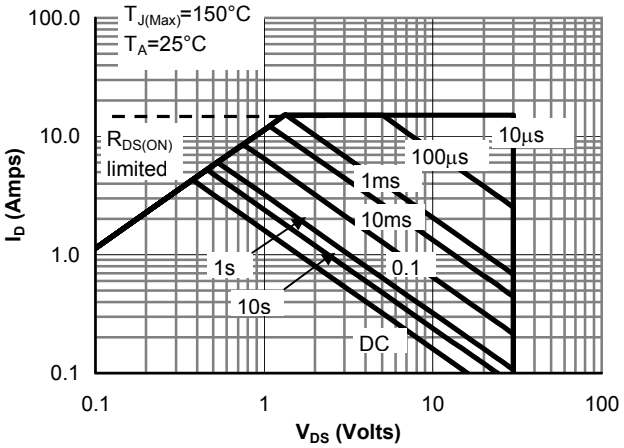


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

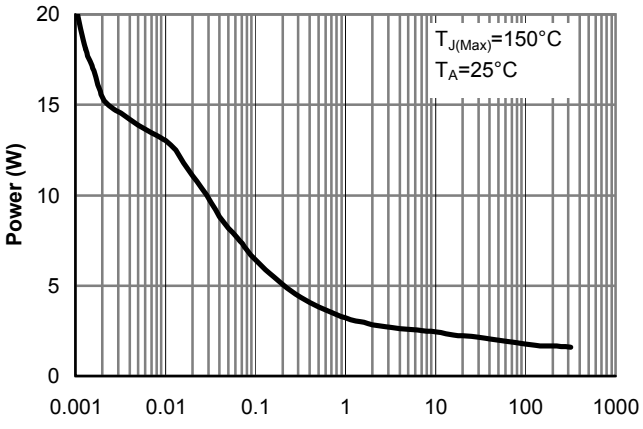


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

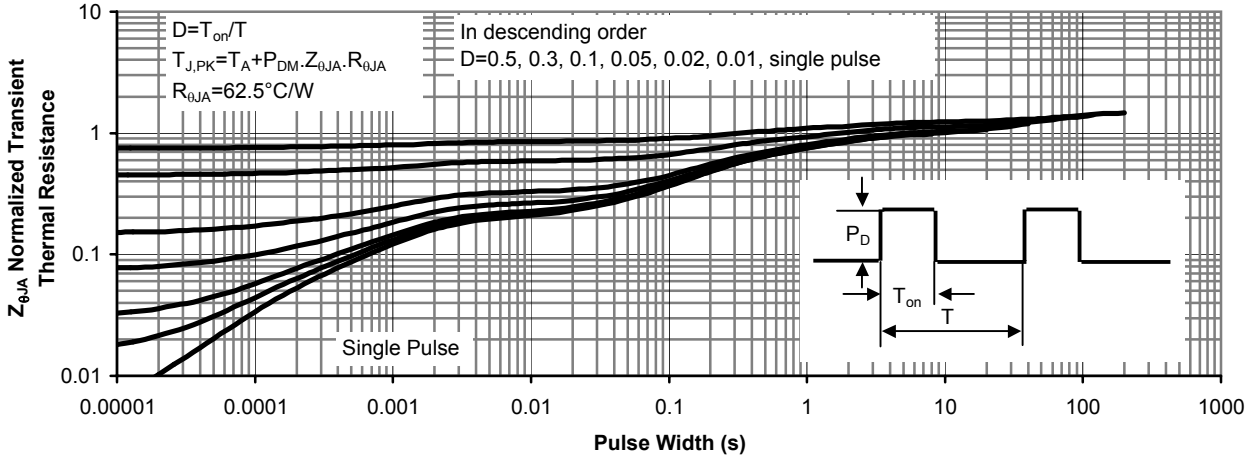


Figure 11: Normalized Maximum Transient Thermal Impedance

p-channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±25V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.7	-2.5	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-8A		16	19	mΩ
		T_J=125°C		20.5	25	
		V_{GS}=-20V, I_D=-8A		15	18	mΩ
		V_{GS}=-4.5V, I_D=-5A		33		mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-8A	16	21		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.6	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		2076		pF
C_{oss}	Output Capacitance			503		pF
C_{rss}	Reverse Transfer Capacitance			302		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-8A		39		nC
Q_{gs}	Gate Source Charge			8		nC
Q_{gd}	Gate Drain Charge			11.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=1.8Ω, R_{GEN}=3Ω		12.7		ns
t_r	Turn-On Rise Time			7		ns
$t_{D(off)}$	Turn-Off DelayTime			25.2		ns
t_f	Turn-Off Fall Time			12		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-8A, dI/dt=100A/µs		32		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-8A, dI/dt=100A/µs		26		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev 3 : Sept 2005

P-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

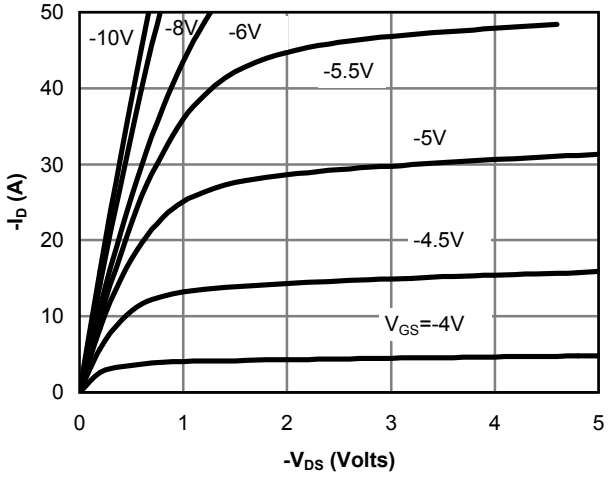


Fig 1: On-Region Characteristics

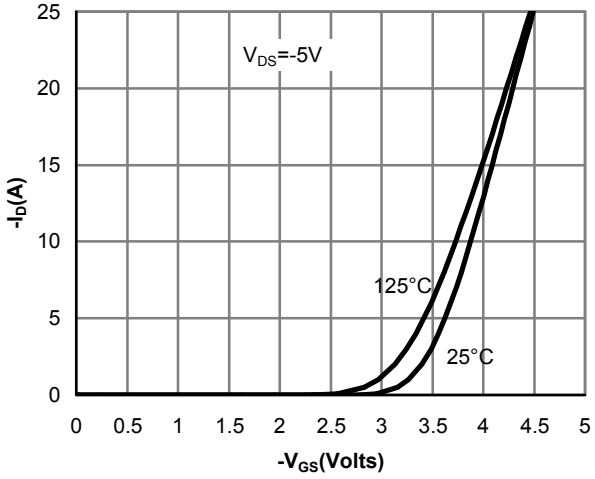


Figure 2: Transfer Characteristics

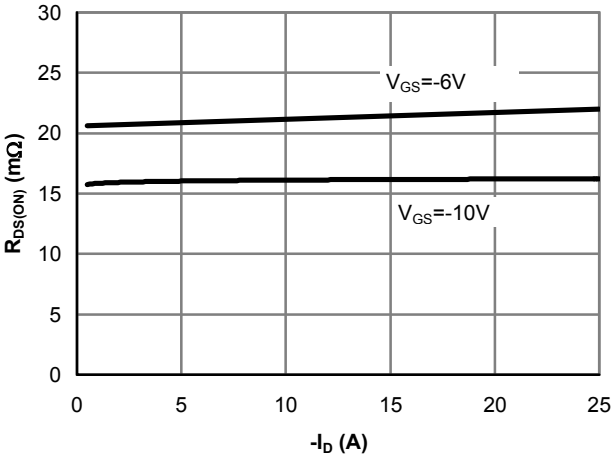


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

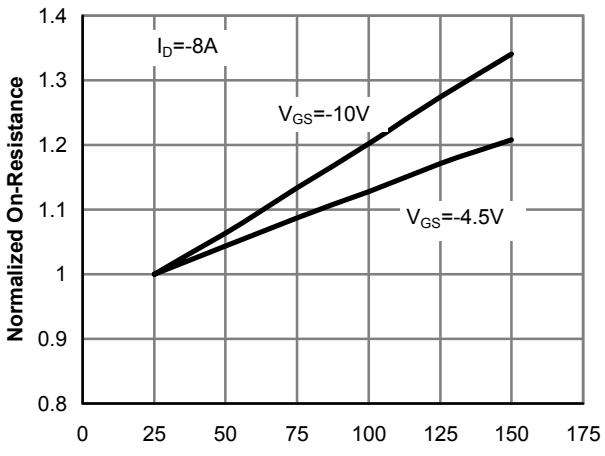


Figure 4: On-Resistance vs. Junction Temperature

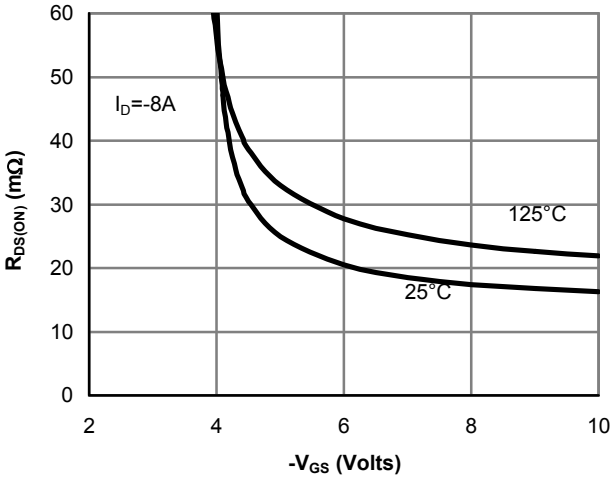


Figure 5: On-Resistance vs. Gate-Source Voltage

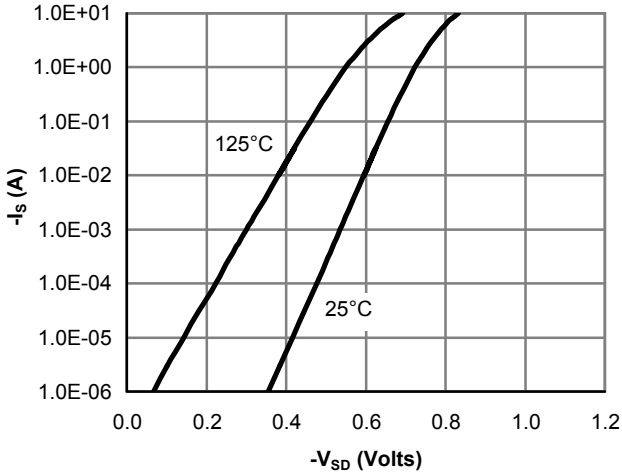


Figure 6: Body-Diode Characteristics

P-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

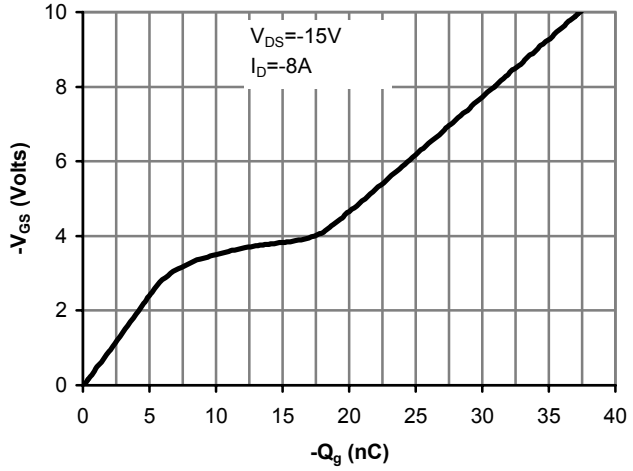


Figure 7: Gate-Charge Characteristics

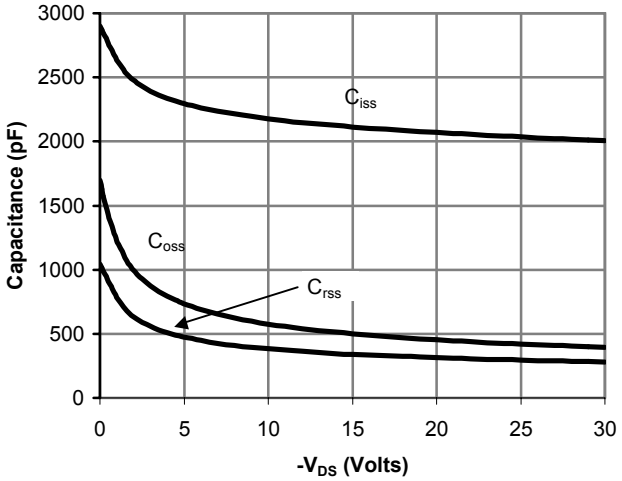


Figure 8: Capacitance Characteristics

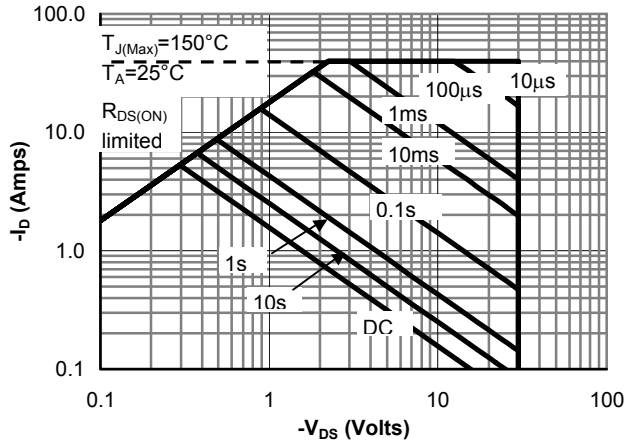


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

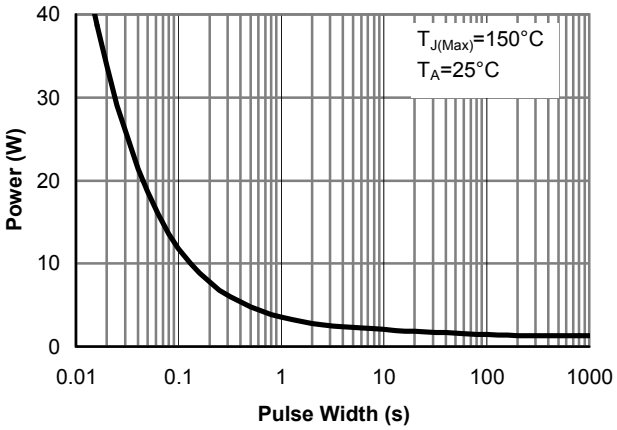


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

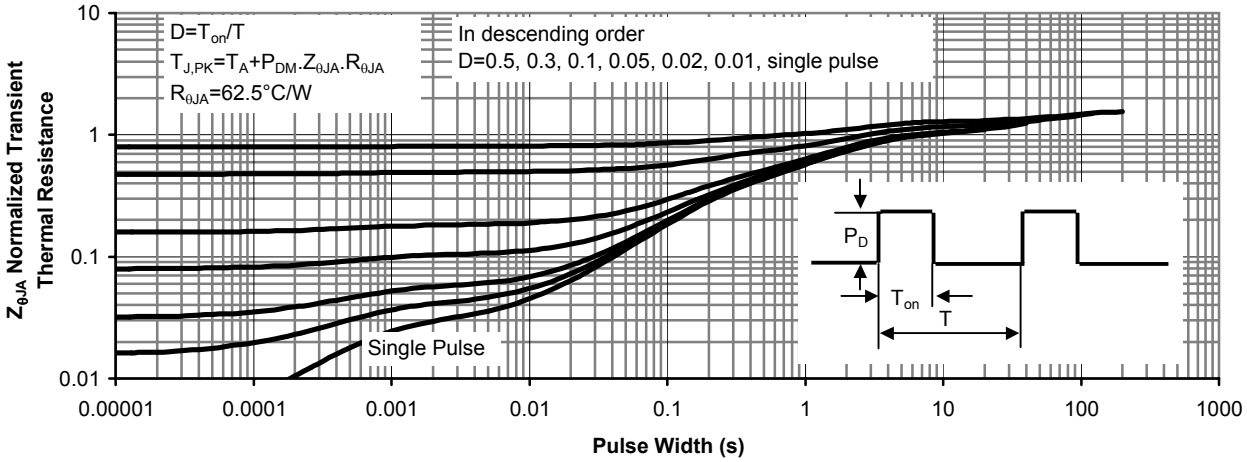


Figure 11: Normalized Maximum Transient Thermal Impedance