



**AOP605**

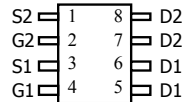
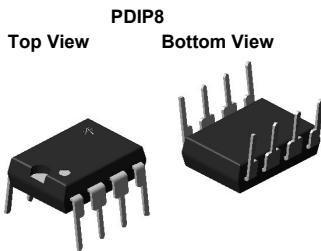
**Complementary Enhancement Mode Field Effect Transistor**

**General Description**

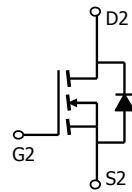
The AOP605/L uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications. AOP605 and AOP605L are electrically identical.  
-RoHS Compliant  
-AOP605L is Halogen Free

**Features**

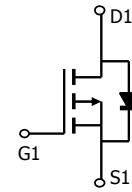
n-channel	p-channel
$V_{DS} (V) = 30V$	-30V
$I_D = 7.5A (V_{GS} = 10V)$	-6.6A ( $V_{GS} = -10V$ )
$R_{DS(ON)}$	
$< 28m\Omega (V_{GS} = 10V)$	$< 35m\Omega (V_{GS} = -10V)$
$< 43m\Omega (V_{GS} = 4.5V)$	$< 58m\Omega (V_{GS} = -4.5V)$



PDIP-8



n-channel



p-channel

**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current <sup>A</sup>	$I_D$	$T_A=25^\circ C$	7.5	-6.6
		$T_A=70^\circ C$	6	-5.3
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	30	-30	A
Power Dissipation	$P_D$	$T_A=25^\circ C$	2.5	2.5
		$T_A=70^\circ C$	1.6	1.6
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ C$

**Thermal Characteristics: n-channel**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	40	50
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	67	80
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	33	40	$^\circ C/W$

**Thermal Characteristics: p-channel**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	38	50
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	66	80
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	30	40	$^\circ C/W$

n-channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.8	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =7.5A T <sub>J</sub> =125°C		22.6	28	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =6.0A		33	43	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =7.5A	12	16		S
V <sub>SD</sub>	Body Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.76	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		680	820	pF
C <sub>oss</sub>	Output Capacitance			102		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			77		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		1.2	2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =7.5A		13.84	16.6	nC
Q <sub>g</sub>	Total Gate Charge			6.74	8.1	nC
Q <sub>gs</sub>	Gate Source Charge			1.82		nC
Q <sub>gd</sub>	Gate Drain Charge			3.2		nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =2.0Ω, R <sub>GEN</sub> =6Ω		4.6		ns
t <sub>r</sub>	Turn-On Rise Time			4.1		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			20.6		ns
t <sub>f</sub>	Turn-Off Fall Time			5.2		ns
t <sub>rr</sub>	Body Diode Reverse Recovery time	I <sub>F</sub> =7.5A, di/dt=100A/μs		16.5	20	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery charge	I <sub>F</sub> =7.5A, di/dt=100A/μs		7.8		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t<sub>θJA</sub> ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

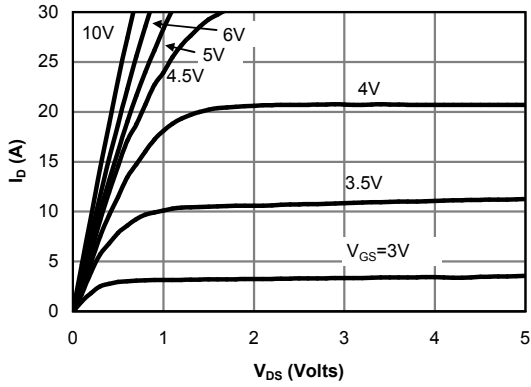


Fig 1: On-Region Characteristics

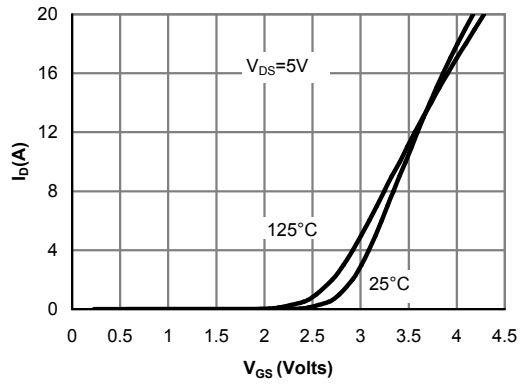


Figure 2: Transfer Characteristics

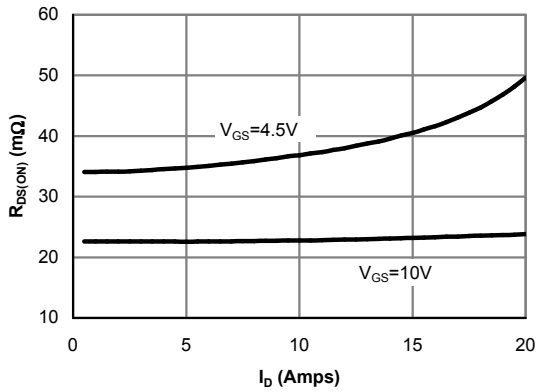


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

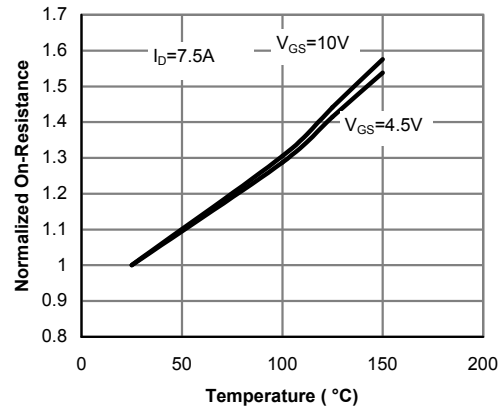


Figure 4: On-Resistance vs. Junction Temperature

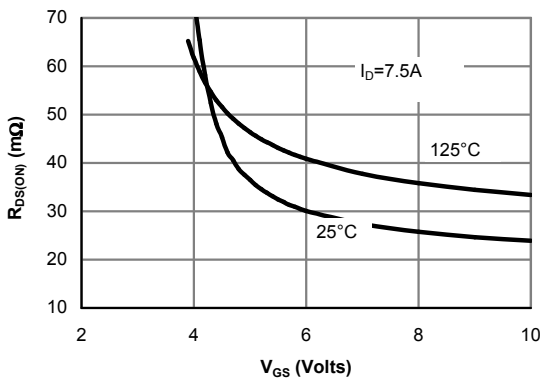


Figure 5: On-Resistance vs. Gate-Source Voltage

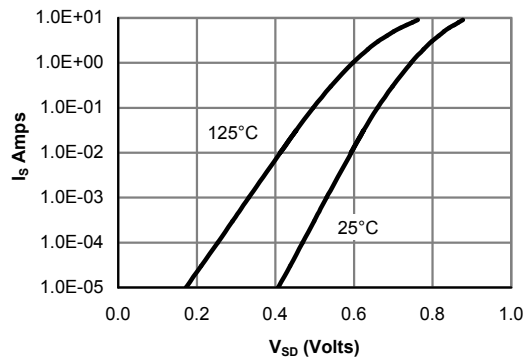


Figure 6: Body diode characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

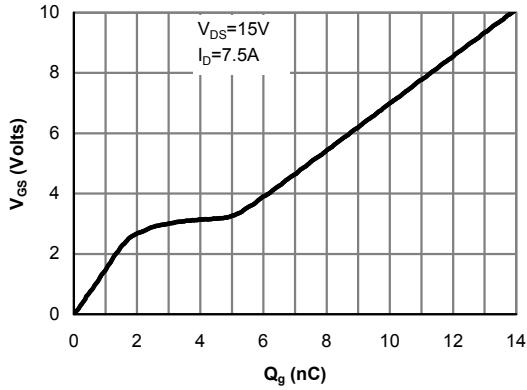


Figure 7: Gate-Charge characteristics

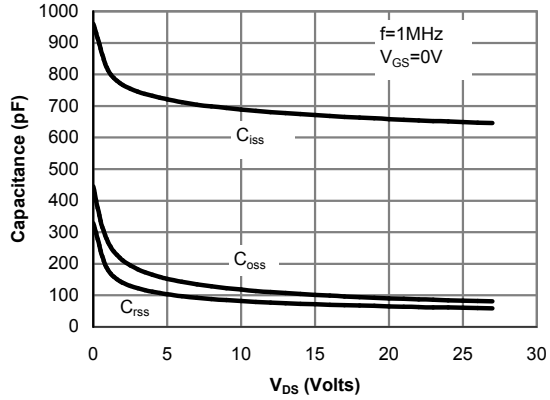


Figure 8: Capacitance Characteristics

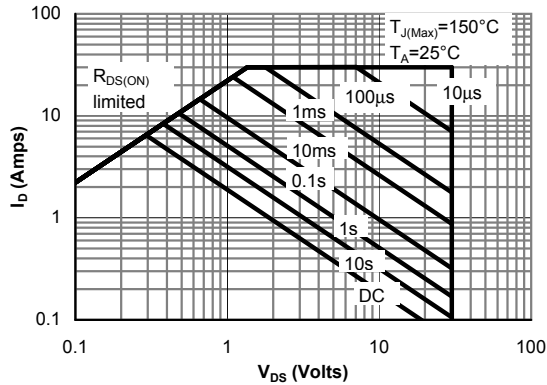


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

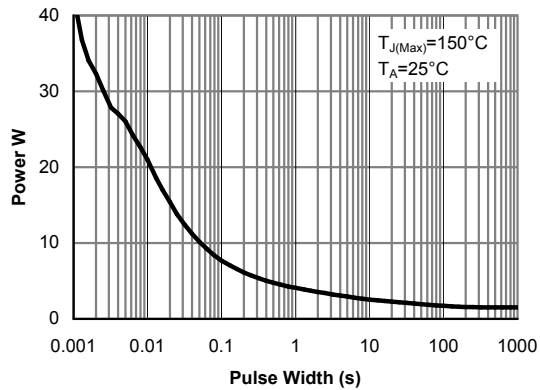


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

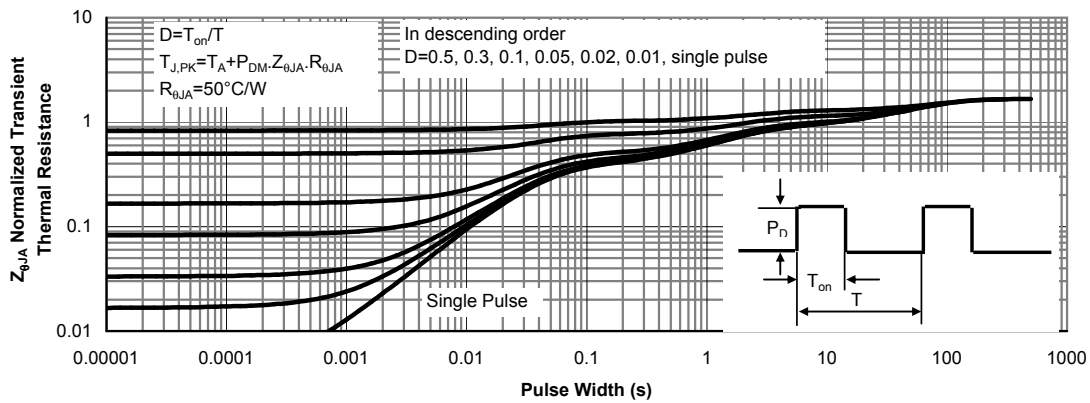
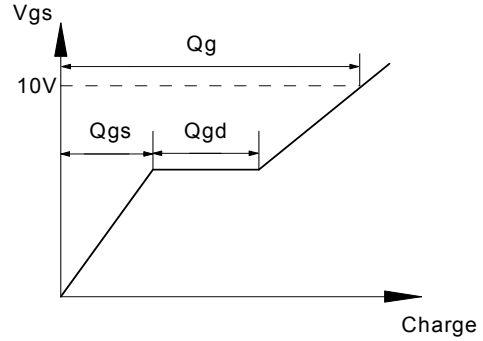
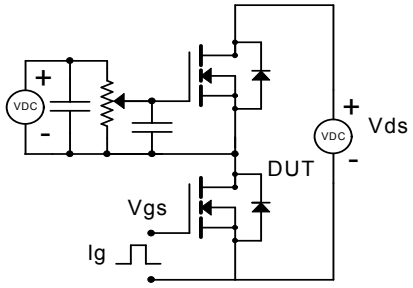
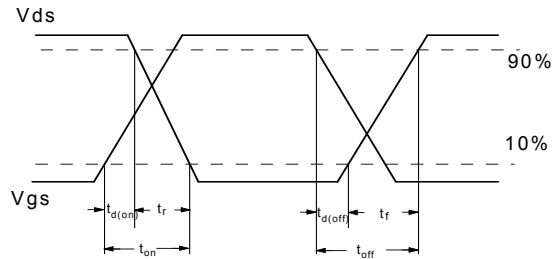
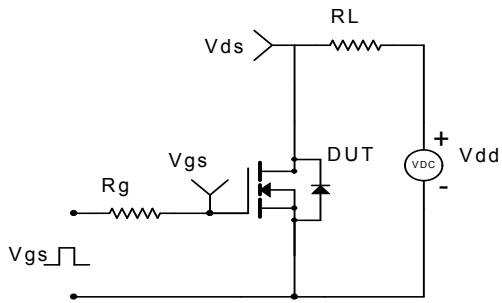


Figure 11: Normalized Maximum Transient Thermal Impedance

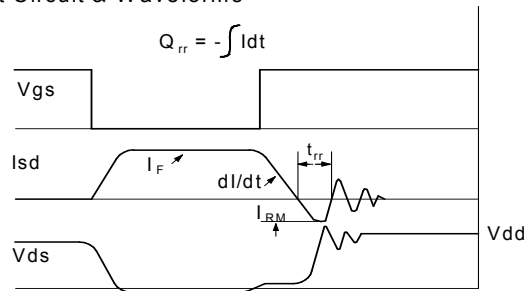
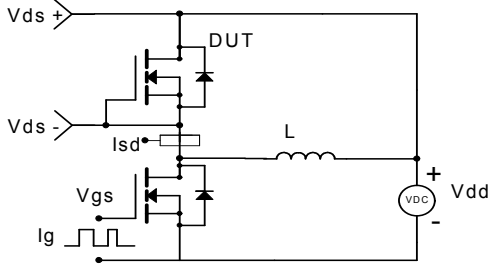
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



p-channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-24\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.2	-2	-2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}, V_{DS}=-5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=-6.6\text{A}$ $T_J=125^\circ\text{C}$		28 37	35 45	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-5\text{A}$		44	58	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-6.6\text{A}$		13		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.76	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-4.2	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1\text{MHz}$		920	1100	pF
$C_{oss}$	Output Capacitance			190		pF
$C_{rss}$	Reverse Transfer Capacitance			122		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		3.6	4.4	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, I_D=-6.6\text{A}$		18.5	22.2	nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			9.6	11.6	nC
$Q_{gs}$	Gate Source Charge			2.7		nC
$Q_{gd}$	Gate Drain Charge			4.5		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, R_L=2.3\Omega,$ $R_{GEN}=3\Omega$		7.7		ns
$t_r$	Turn-On Rise Time			5.7		ns
$t_{D(off)}$	Turn-Off DelayTime			20.2		ns
$t_f$	Turn-Off Fall Time			9.5		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-6.6\text{A}, dI/dt=100\text{A}/\mu\text{s}$		20	24	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-6.6\text{A}, dI/dt=100\text{A}/\mu\text{s}$		8.8		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80  $\mu\text{s}$  pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

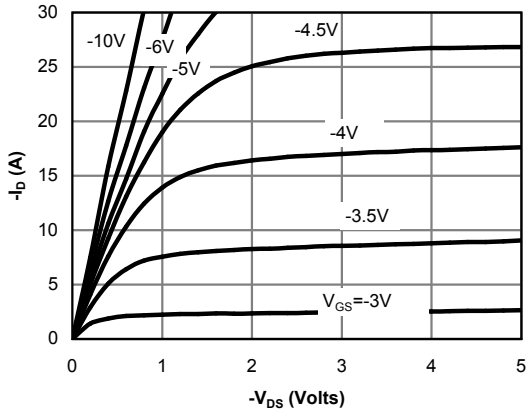


Fig 1: On-Region Characteristics

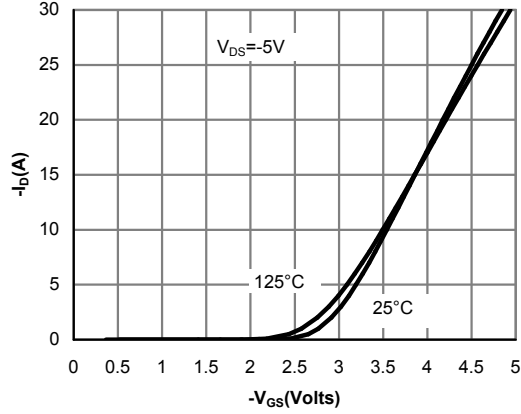


Figure 2: Transfer Characteristics

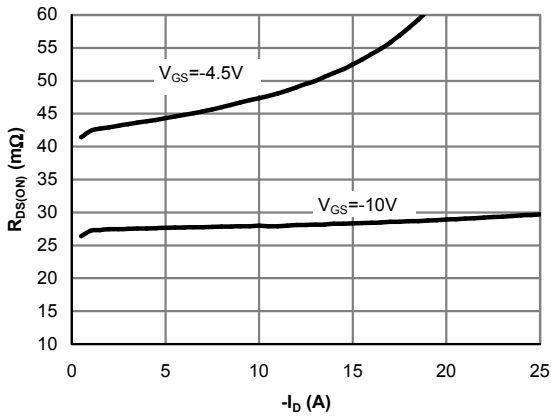


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

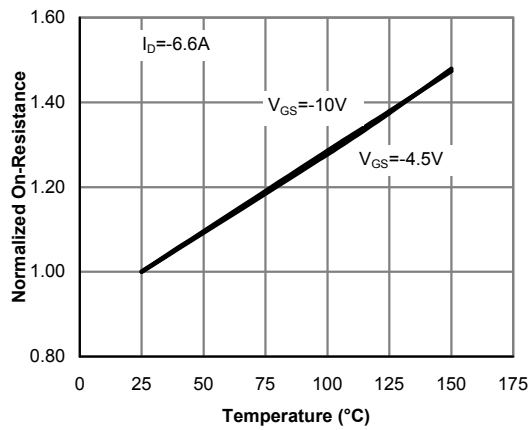


Figure 4: On-Resistance vs. Junction Temperature

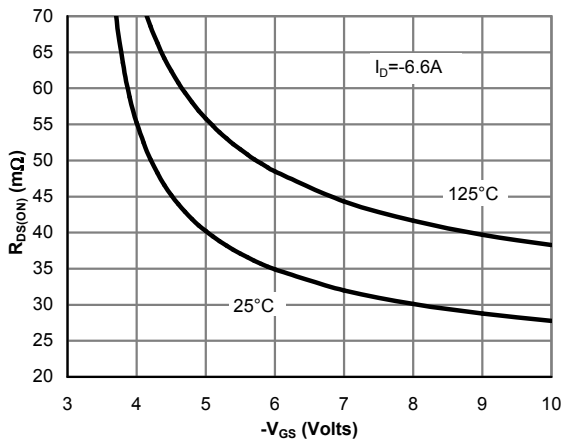


Figure 5: On-Resistance vs. Gate-Source Voltage

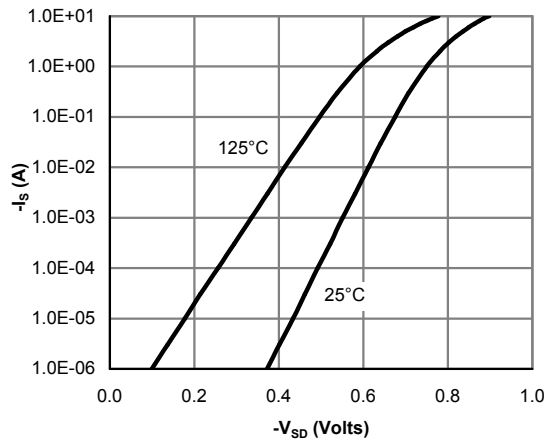


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

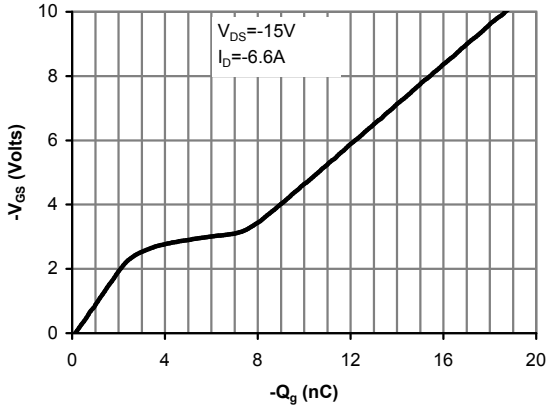


Figure 7: Gate-Charge Characteristics

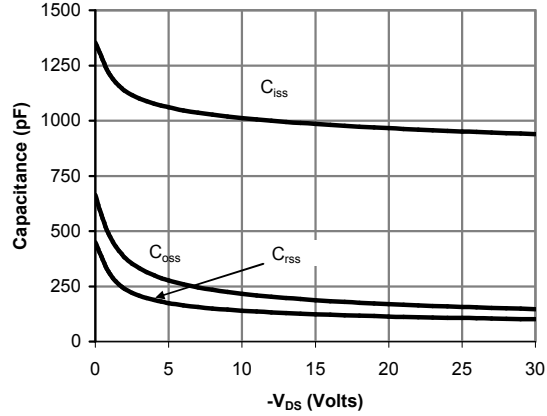


Figure 8: Capacitance Characteristics

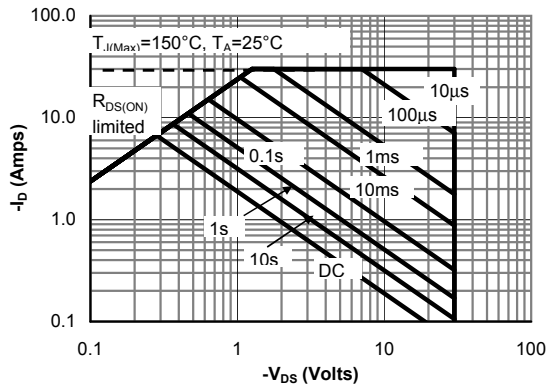


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

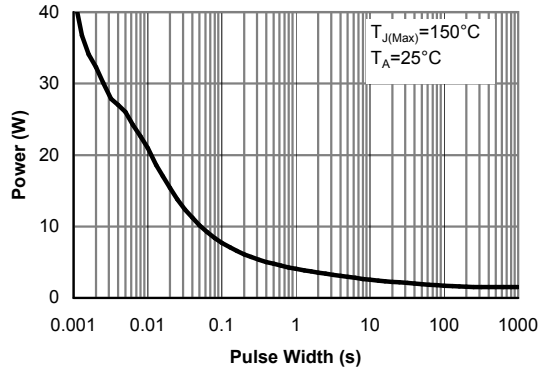


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

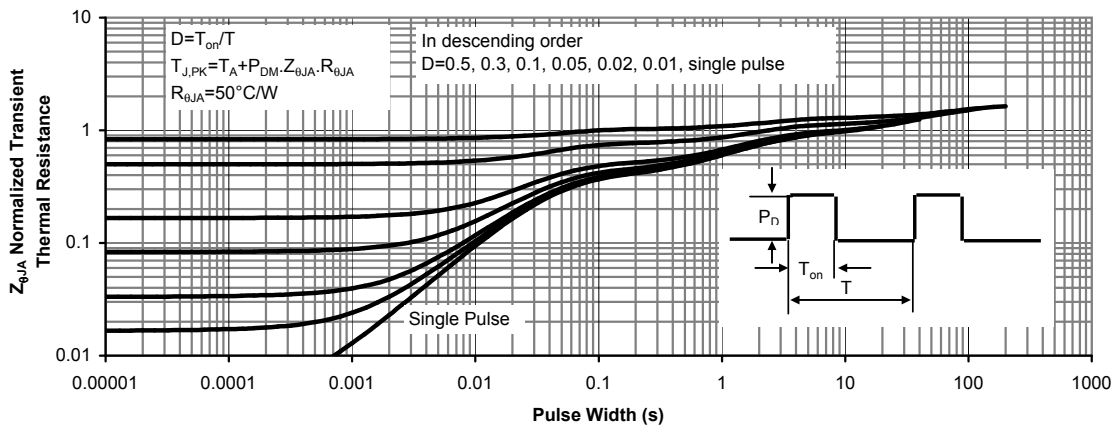
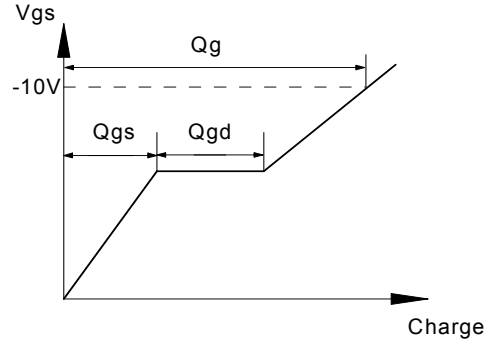
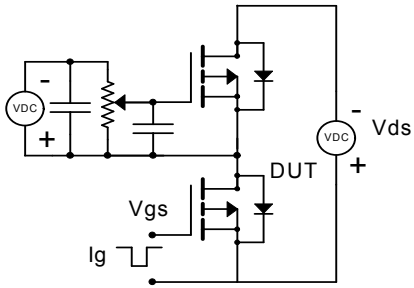


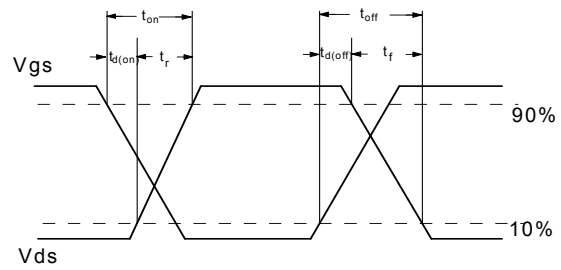
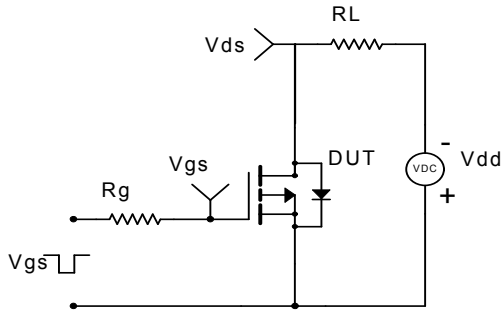
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Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

