N-channel enhancement mode vertical D-MOS transistor

BSN20

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a surface-mounted device in thin and thick film circuits and in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	100	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

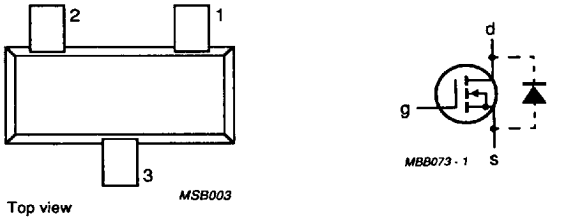

Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	300	mW
		up to T_{amb} = 25 °C (note 2)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430 K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500 K/W

Notes

1. Transistor mounted on a ceramic substrate, 10 x 8 x 0.7 mm.
2. Transistor mounted on a printed circuit board.

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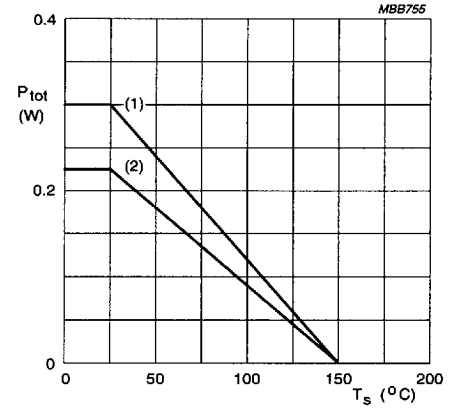
CHARACTERISTICS

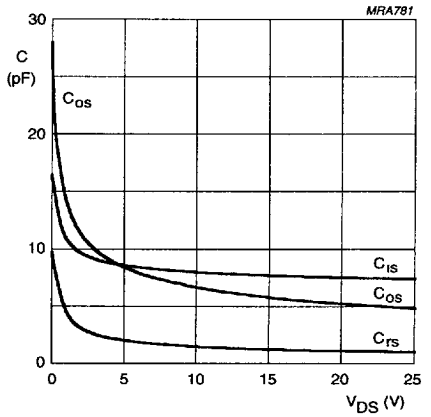
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	8	15	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	14	20	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	18	30	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	40	80	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	7	15	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	5	10	ns



(1) Mounted on a ceramic substrate.
(2) Mounted on a printed circuit board.

Fig.2 Power derating curve.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.3 Capacitance as a function of drain-source voltage, typical values.

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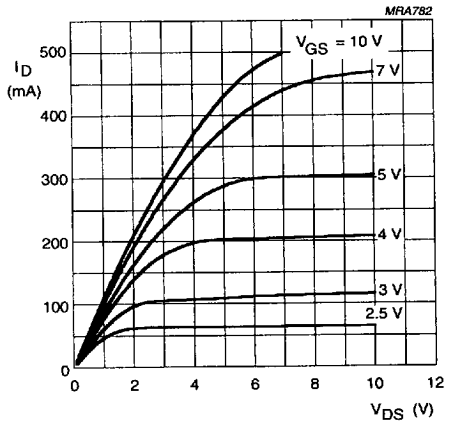
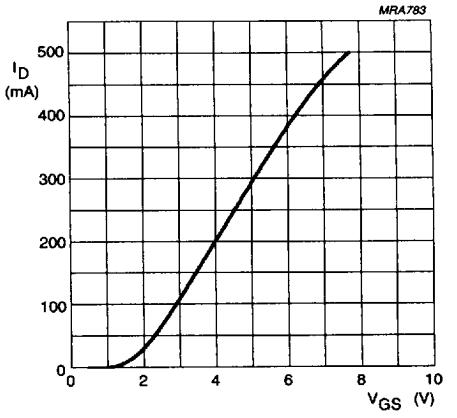


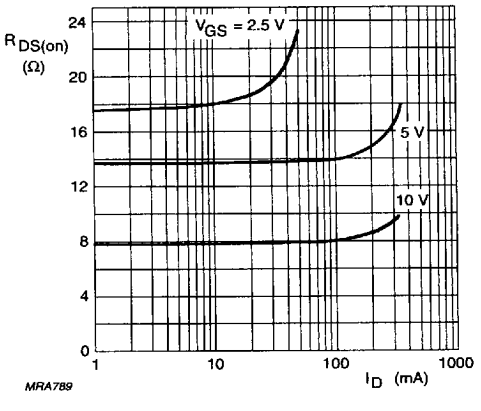
T_j = 25 °C.

Fig.4 Typical output characteristics.



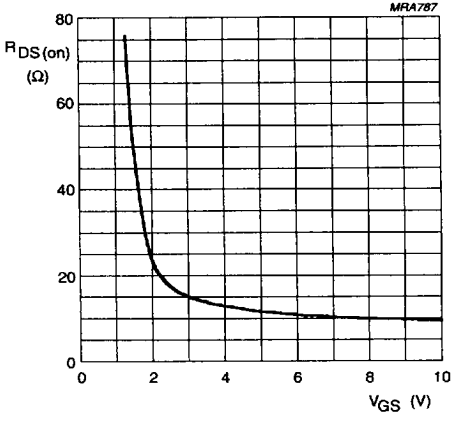
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



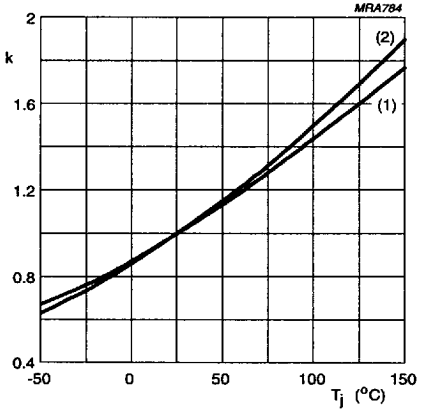
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



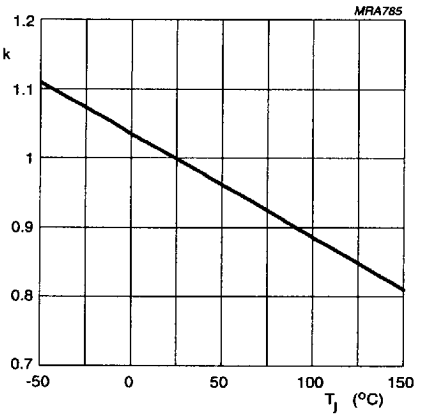
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$ at 100 mA/10 V.

(1) I_D = 10 mA; V_{GS} = 2.5 V.

(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage.