Data sheet acquired from Harris Semiconductor
SCHS138C

# CD74HC93, CD74HCT93

## High-Speed CMOS Logic 4-Bit Binary Ripple Counter

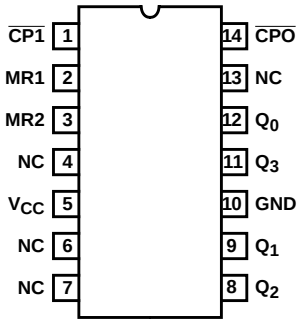
August 1997 - Revised September 2003

### Features

- **Can Be Configured to Divide By 2, 8, and 16**
- **Asynchronous Master Reset**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{o}$C to 125$^{o}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Pinout

**CD74HC93**
**(PDIP, SOIC)**
**CD74HCT93**
**(PDIP)**
TOP VIEW




### Description

The CD74HC93 and CD74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide- by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH to LOW clock transition. State changes of the $Q_n$ outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR1 and MR2 is provided which overrides both clocks and resets (clears) all flip-flops.

Because the output from the divide by two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output $Q_0$ must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the $Q_0$, $Q_1$, $Q_2$, and $Q_3$ outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the $Q_1$, $Q_2$, $Q_3$ outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE |
|---|---|---|
| CD74HC93E | -55 to 125 | 14 Ld PDIP |
| CD74HC93M | -55 to 125 | 14 Ld SOIC |
| CD74HC93MT | -55 to 125 | 14 Ld SOIC |
| CD74HC93M96 | -55 to 125 | 14 Ld SOIC |
| CD74HCT93E | -55 to 125 | 14 Ld PDIP |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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**TRUTH TABLE**

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

H = High Voltage Level, L = Low Voltage Level

**MODE SELECTION**

| RESET OUTPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| MR1 | MR2 | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| H | H | L | L | L | L |
| L | H | Count | Count | Count | Count |
| H | L | | | | |
| L | L | | | | |

H = High Voltage Level, L = Low Voltage Level

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| E (PDIP) Package | 80 |
| M (SOIC) Package | 86 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| $\overline{CP0}$, $\overline{CP1}$ | 0.6 |
| MR1, MR2 | 0.4 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | |
| Maximum Clock Frequency | $f_{MAX}$ | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| Clock Pulse Width $\overline{CP0}$, $\overline{CP1}$ | $t_W$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |

## Prerequisite For Switching Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Reset Pulse Width | $t_W$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Reset Removal Time | $t_{REM}$ | 2 | 50 | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | 11 | - | 13 | - | ns |
| **HCT TYPES** | | | | | | | | | |
| Maximum Clock Frequency | $f_{MAX}$ | 4.5 | 30 | - | 24 | - | 20 | - | mHz |
| Clock Pulse Width $\overline{CP0}$, $\overline{CP1}$ | $t_W$ | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| Reset Pulse Width | $t_W$ | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| Reset Removal Time | $t_{REM}$ | 4.5 | 10 | - | 13 | - | 15 | - | ns |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| $\overline{CP0}$ to Q0 | | $C_L$ = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | $C_L$ = 15pF | 5 | - | 10 | | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| $\overline{CP1}$ to Q1 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | | 135 | - | 170 | - | 205 | ns |
| | | $C_L$ = 50pF | 4.5 | - | | 27 | - | 34 | - | 41 | ns |
| | | $C_L$ = 50pF | 6 | - | | 23 | - | 29 | - | 35 | ns |
| $\overline{CP1}$ to Q2 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | | 185 | - | 230 | - | 280 | ns |
| | | $C_L$ = 50pF | 4.5 | - | | 37 | - | 46 | - | 56 | ns |
| | | $C_L$ = 50pF | 6 | - | | 31 | - | 39 | - | 48 | ns |
| $\overline{CP1}$ to Q3 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | | 245 | - | 305 | - | 370 | ns |
| | | $C_L$ = 50pF | 4.5 | - | | 49 | - | 61 | - | 74 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 42 | - | 52 | - | 63 | ns |
| MR1, MR2 to Qn | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | | 155 | - | 195 | - | 235 | ns |
| | | $C_L$ = 50pF | 4.5 | - | | 31 | - | 39 | - | 47 | ns |
| | | $C_L$ = 15pF | 5 | - | 13 | | - | | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | | 26 | - | 33 | - | 40 | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | - | - | - | 25 | - | - | 10 | - | 19 | pF |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| $\overline{CP0}$ to Q0 | | $C_L$ = 15pF | 5 | - | 14 | - | - | - | - | - | ns |
| $\overline{CP1}$ to Q1 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| | | $C_L$ = 15pF | 5 | - | - | - | - | - | - | - | ns |
| $\overline{CP1}$ to Q2 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 46 | - | 58 | - | 69 | ns |
| | | $C_L$ = 15pF | 5 | - | - | - | - | - | - | - | ns |
| $\overline{CP1}$ to Q3 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 58 | - | 73 | - | 87 | ns |
| | | $C_L$ = 15pF | 5 | - | 24 | - | - | - | - | - | ns |
| MR1, MR2 to Qn | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 33 | - | 41 | - | 50 | ns |
| | | $C_L$ = 15pF | 5 | - | 13 | - | - | - | - | - | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | - | - | - | - | 25 | - | - | - | - | pF |

## *Test Circuits and Waveforms*

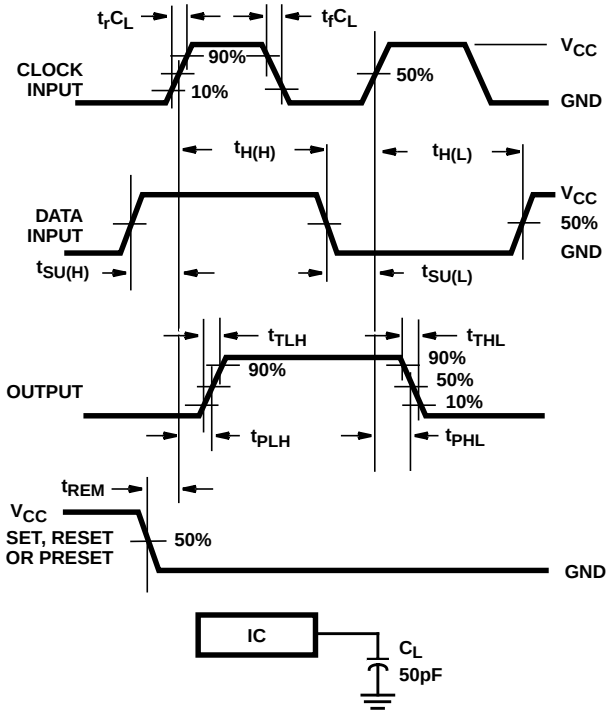


**FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

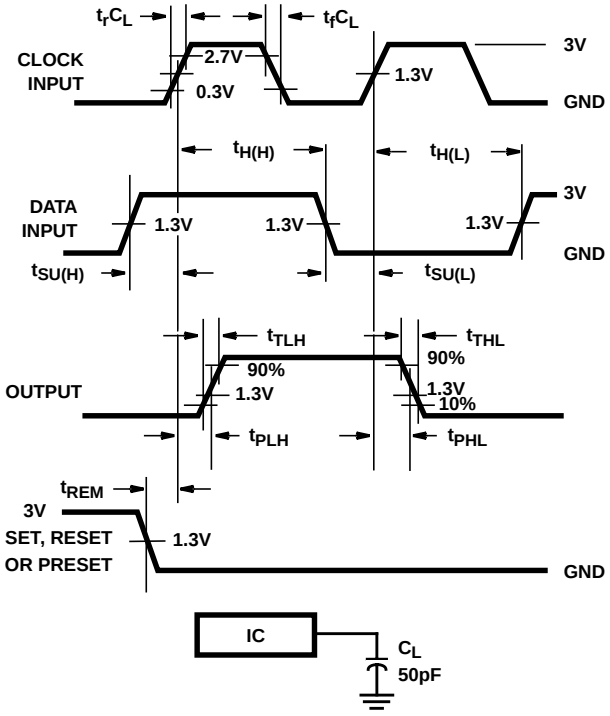


**FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CD74HC93E | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD74HC93EE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD74HC93M | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD74HC93M96 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD74HC93M96E4 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD74HC93ME4 | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD74HC93MT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD74HC93MTE4 | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD74HCT93E | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD74HCT93EE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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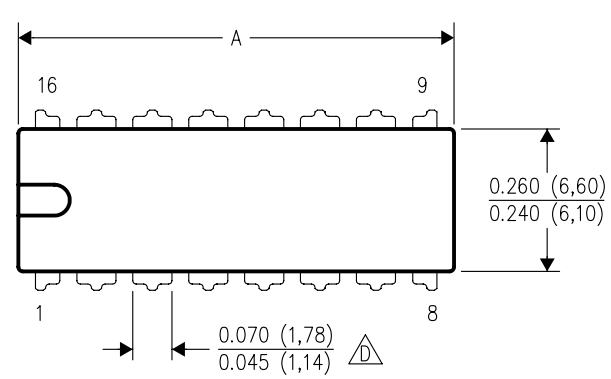
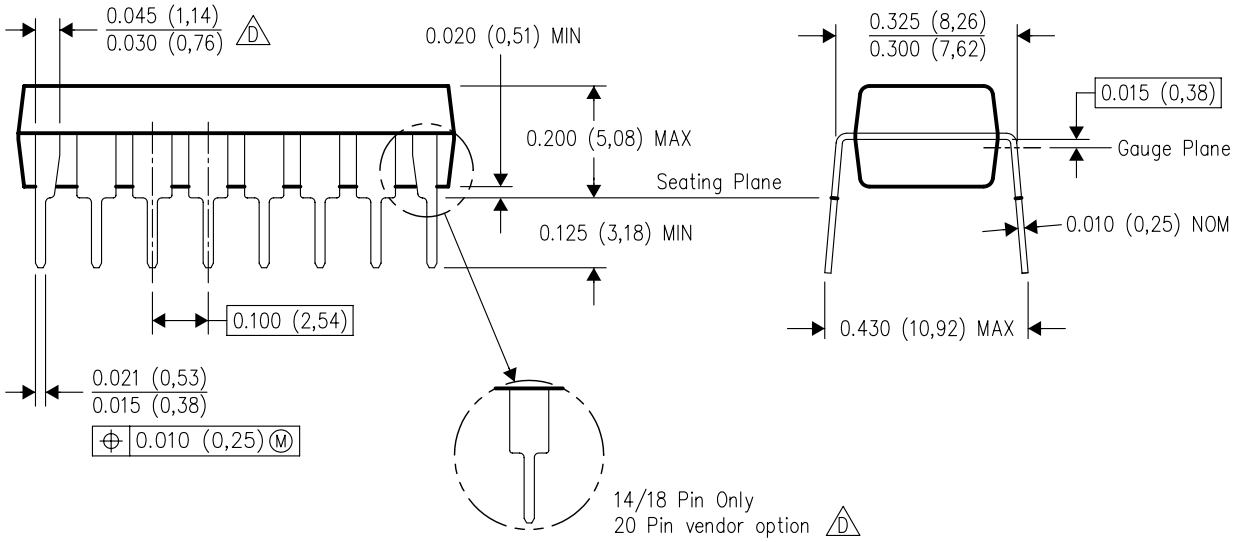
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

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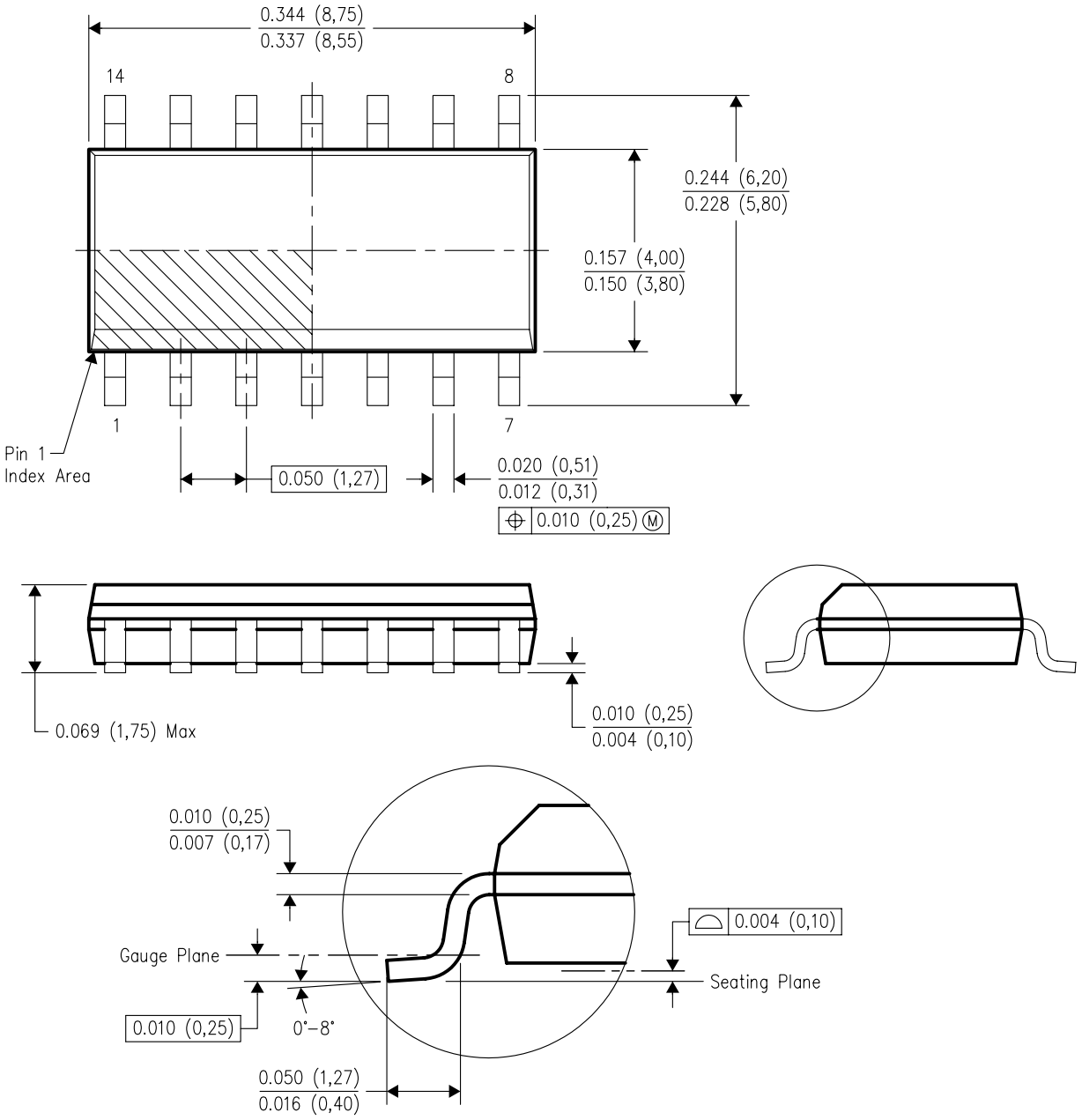
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

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