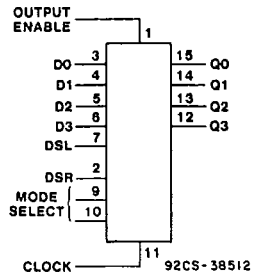
File Number 1661

CD54/74HC40104
CD54/74HCT40104

T-46-09-05

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

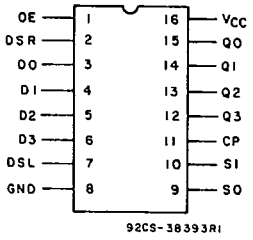
4-Bit Universal Bidirectional Shift Register

Type Features:
- *Four operating modes: shift right, shift left, hold and reset*
- *Three-state outputs*
- *Synchronous parallel or serial operation*
- *Typical f_{MAX}=50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC40104 and CD54/74HCT40104 are 4-bit shift registers with 3-state bus interface capability. In the parallel mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input. During parallel loading serial data flow is inhibited. Shift left and Shift right are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and the SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state.

The CD54HC/HCT40104 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT40104 are supplied in 16-lead plastic dual-in-line packages (E suffix), also in 16-lead surface mount plastic dual-in-line packages (M suffix). These types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

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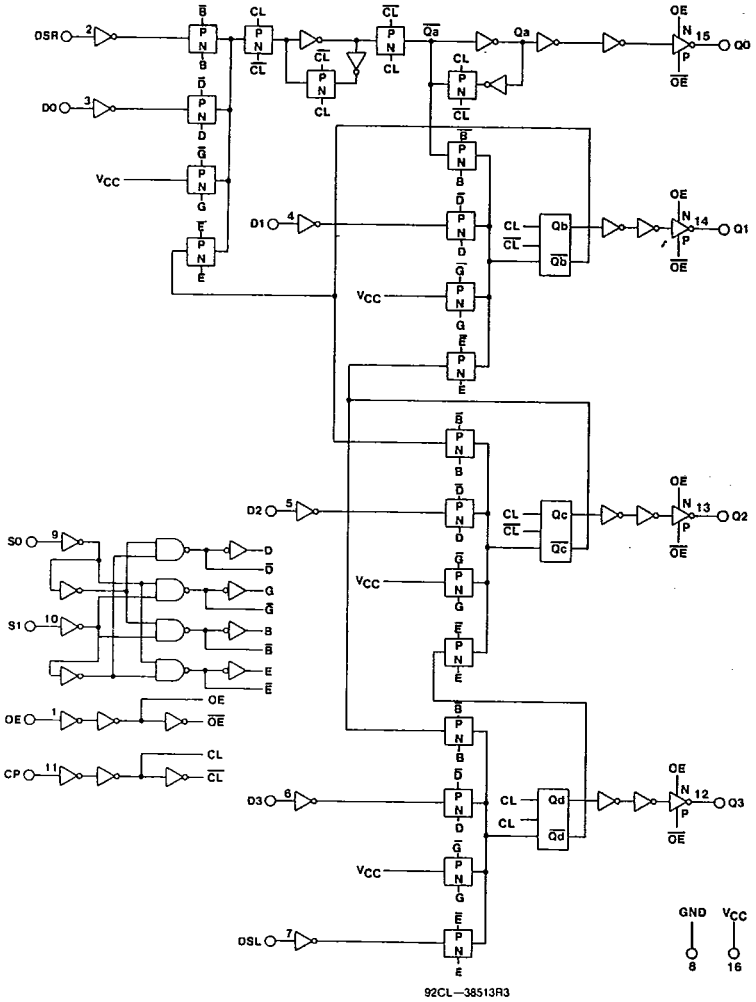

Fig. 1 - Logic diagram.

TRUTH TABLE

CLOCK	MODE SELECT S0	MODE SELECT S1	OUTPUT ENABLE OE	ACTION
⎍	L	L	H	Reset
⎍	H	L	H	Shift right (Q0 toward Q3)
⎍	L	H	H	Shift left (Q3 toward Q0)
⎍	H	H	H	Parallel load
X	X	X	L	Operations occur as shown above, but outputs assume high impedance

L = Low Voltage Level

H = High Voltage Level

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < 0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) ..... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -65 to +150°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC40104/CD54HC40104										CD74HCT40104/CD54HCT40104									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

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HCT Input Loading Table

Input	Unit Loads*
OE	1.4
DSR, DSL, D0-D3	0.3
S1, S2	0.7
CP	0.3

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Maximum Frequency (C_L = 15 pF)	f_{MAX}	56	50	MHz
Propagation Delay: (C_L = 15 pF) CP to Qn	t_{PLH} t_{PHL}	17	18	ns
Output Disable Time	t_{PLZ} t_{PHZ}	14	18	ns
Output Enable Time	t_{PZL} t_{PZH}	12	12	ns
Power Dissipation Capacitance	C_{PD}*	84	85	pF

*C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	28	—	25	—	22	—	20	—	19	—	17	—	
		6	33	—	—	—	26	—	—	—	22	—	—	—	
Clock Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Times Dn, DSL, DSR, S1, and S0 to Clock	t_{su}	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Times Dn, DSO, DSI, S1, and S0 to Clock	t_H	2	2	—	—	—	2	—	—	—	2	—	—	—	
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	

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SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay CP to Qn	t_{PLH} t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	42	—	50	—	53	—	60	—	63	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Disable Time	t_{PLZ} t_{PHZ}	2	—	175	—	—	—	219	—	—	—	263	—	—	
		4.5	—	35	—	44	—	44	—	55	—	53	—	66	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Enable Time	t_{PZL} t_{PZH}	2	—	150	—	—	—	188	—	—	—	225	—	—	
		4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	32	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	

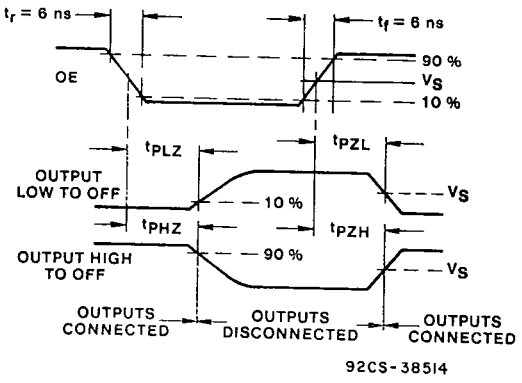

Fig. 2 - Output enable and disable times.

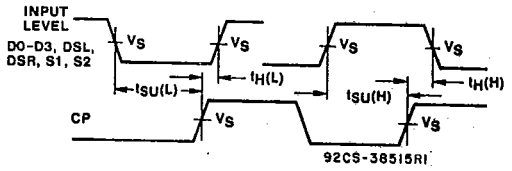

Fig. 3 - Setup and hold times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V