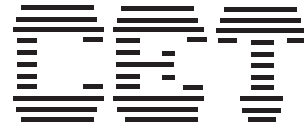


# CEP6030L/CEB6030L



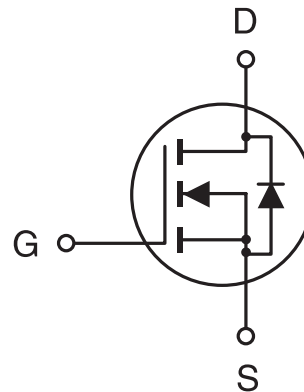
March 1998

4

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

- 30V , 52A ,  $R_{DS(ON)}=13.5m\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=20m\Omega$  @  $V_{GS}=4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Drain Current-Continuous @ $T_J=125^\circ C$ -Pulsed	$I_D$	52	A
	$I_{DM}$	156	A
Drain-Source Diode Forward Current	$I_S$	52	A
Maximum Power Dissipation <sup>a</sup> @ $T_c=25^\circ C$ Derate above $25^\circ C$	$P_D$	75	W
		0.5	W/ $^\circ C$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-65 to 175	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

# CEP6030L/CEB6030L

## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			10	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.6	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =26A		11	13.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =21A		16	20.0	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =10V	60			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =26A		32		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1.0MHz		1200	1800	pF
Output Capacitance	C <sub>OSS</sub>			600	1000	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			350	500	pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =52A, V <sub>GS</sub> =10V R <sub>GEN</sub> =24Ω		6	16	ns
Rise Time	t <sub>r</sub>			120	250	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			40	90	ns
Fall Time	t <sub>f</sub>			105	200	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =52A, V <sub>GS</sub> =10V		35	60	nC
Gate-Source Charge	Q <sub>gs</sub>			8		nC
Gate-Drain Charge	Q <sub>gd</sub>			5		nC

# CEP6030L/CEB6030L

4

## ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS <sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 26A$		0.9	1.3	V

Notes

- a. Pulse Test: Pulse Width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

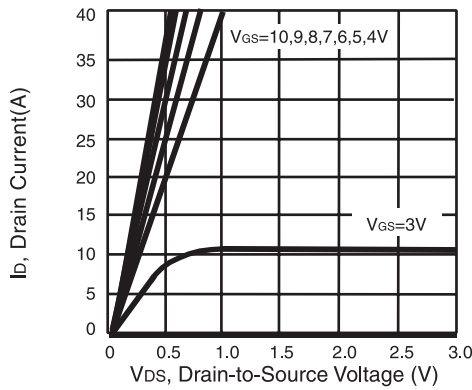


Figure 1. Output Characteristics

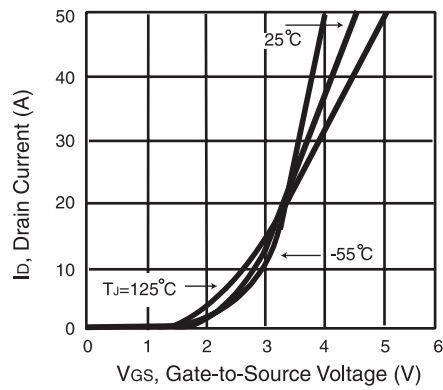


Figure 2. Transfer Characteristics

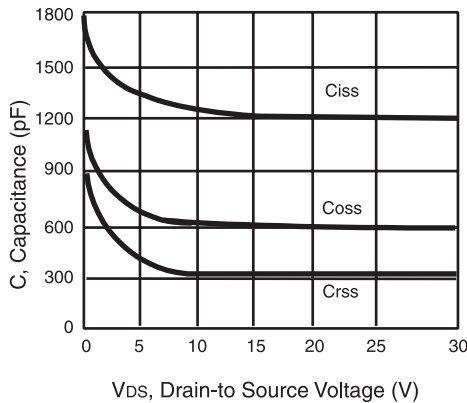


Figure 3. Capacitance

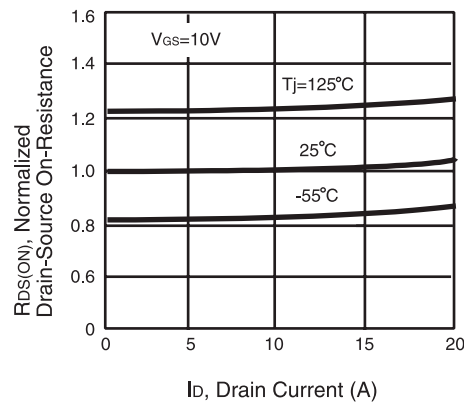
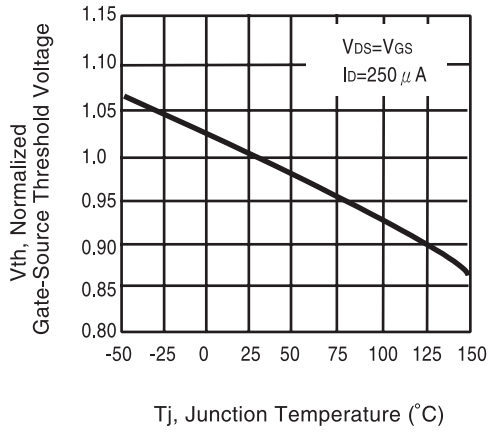
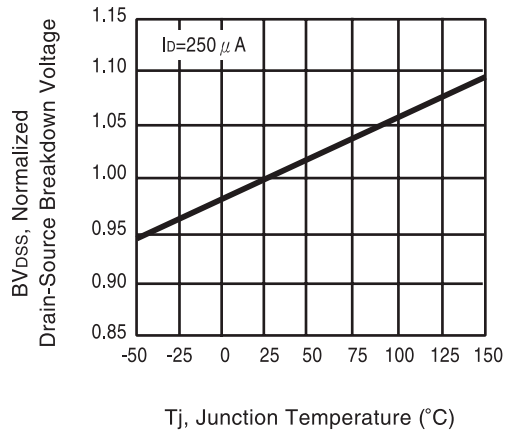


Figure 4. On-Resistance Variation with Drain Current and Temperature

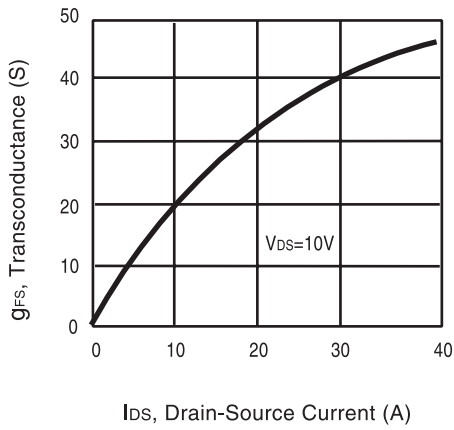
# CEP6030L/CEB6030L



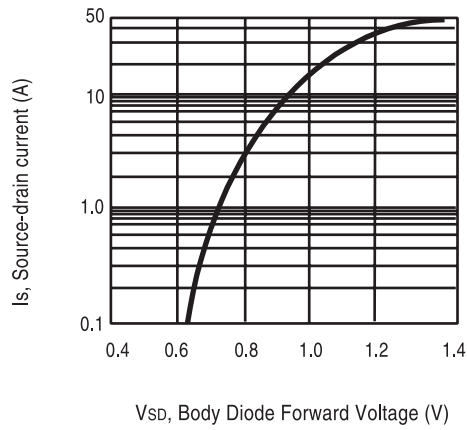
**Figure 5. Gate Threshold Variation with Temperature**



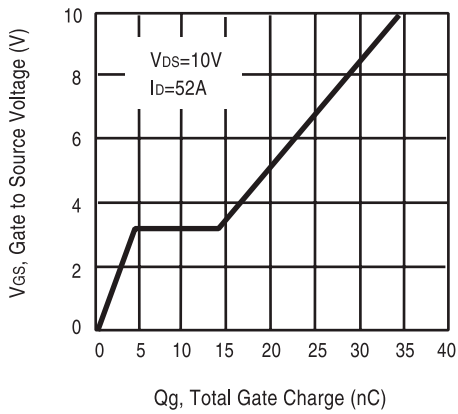
**Figure 6. Breakdown Voltage Variation with Temperature**



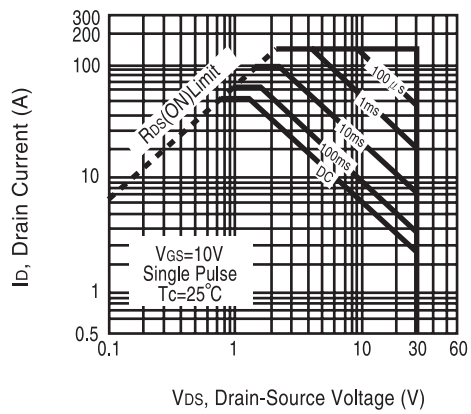
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

# CEP6030L/CEB6030L

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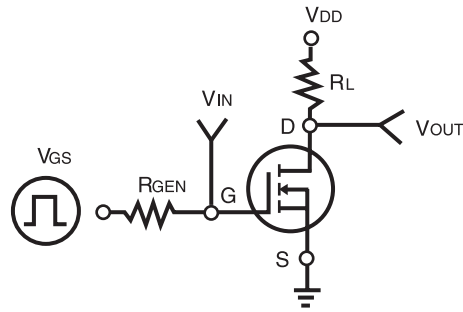


Figure 11. Switching Test Circuit

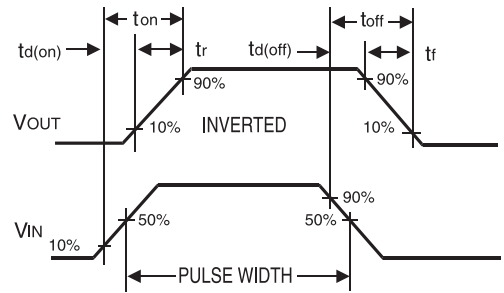


Figure 12. Switching Waveforms

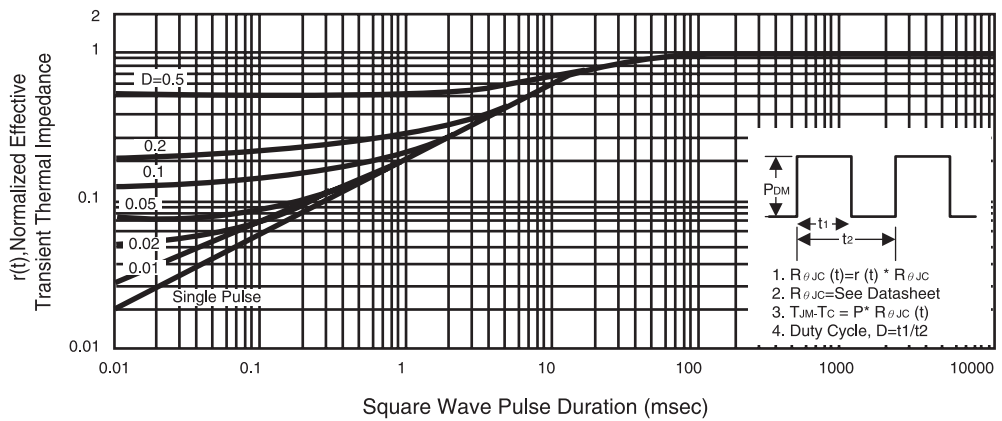


Figure 13. Normalized Thermal Transient Impedance Curve