CR6850D

Novel Low Cost Green-Power PWM Controller

Features

- Low Cost, PWM&PFM&CRM (Cycle Reset Mode)
- Low Start-up Current (about 8μA)
- Low Operating Current (about 2mA)
- Current Mode Operation
- Under Voltage Lockout (UVLO)
- Built-in Synchronized Slope Compensation
- Programmable PWM Frequency
- Audio Noise Free Operation
- Leading edge Blanking on Sense input
- Constant output power limiting for universal AC input
- Cycle-by-cycle current limiting
- Soft clamped gate output voltage 16.8V
- Over voltage protect 25.5V
- High-Voltage CMOS Process with ESD
- SOT-23-6L、SOP-8 & DIP-8 Pb-Free Packaging

Applications

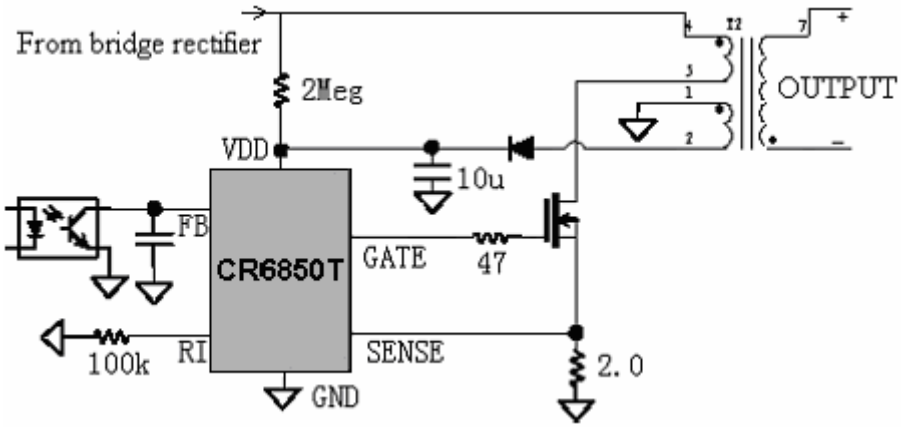
- Switching AC/DC Adaptor
- Battery Charger
- Open Frame Switching Power Supply
- 384X Replacement

General Description

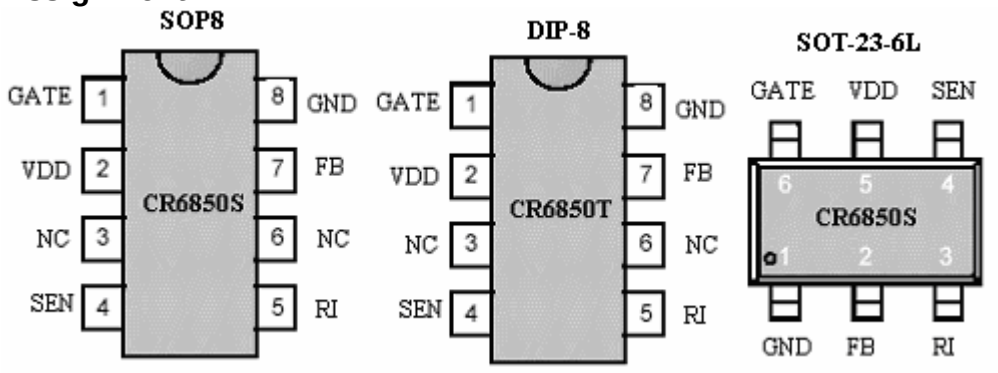
The CR6850D is a highly integrated low cost current mode PWM controller, which is ideal for small power current mode of offline AC-DC fly-back converter applications. Making use of external resistors, the IC changes the operating frequency and automatically enters the PFM/CRM (Cycle Reset Mode) under light-load/zero-load conditions. This can minimize standby power consumption and achieve green-power functions. With a very low start-up current, the CR6850D could use a large value start-up resistor (2Mohm). Built-in synchronized slope compensation enhances the stability of the system and avoids sub-harmonic oscillation. Dynamic peak limiting circuit minimizes output power change caused by delay time of the system over a universal AC input range. Leading edge blanking circuit on current sense input could remove the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. Pulse-by-pulse current limiting ensures safe operation even during short-circuit.

The CR6850D offers more protection like OVP (Over Voltage Protection) and OCP (Over current protection). The CR6850D's output driver is soft clamped to maximum 16.8V to protect the power MOSFET. Excellent EMI performance is achieved soft switching control at the totem pole gate driver output. CR6850D is offered in SOT-23-6, SOT-8 and DIP-8 packages.

TYPICAL APPLICATION



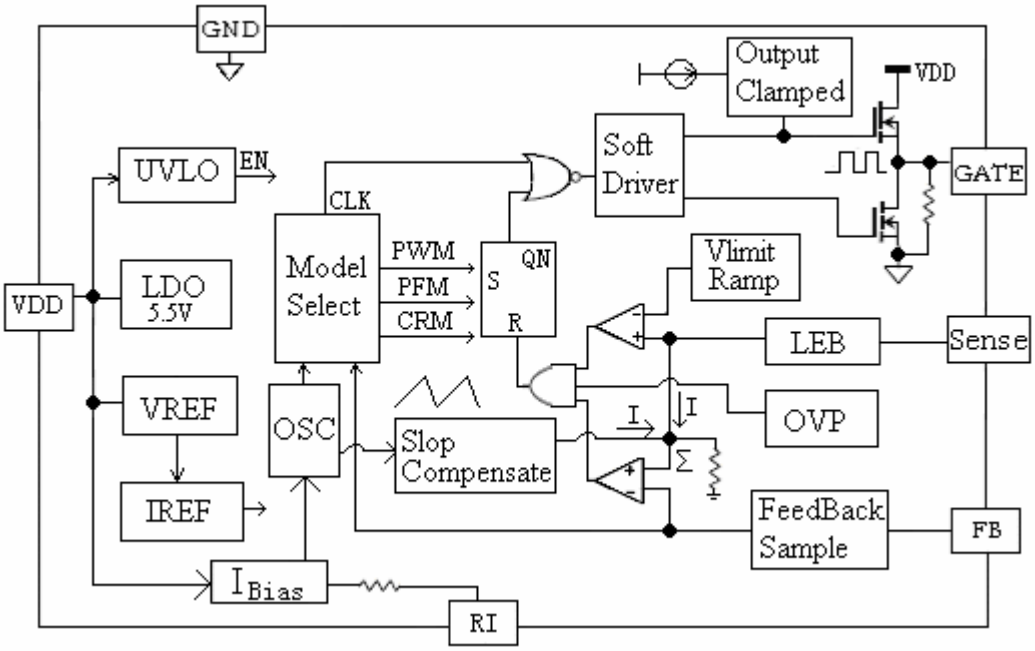
Pin Assignment



Pin Descriptions

Name	Description
GND	GND Pin
FB	Analog Input. Voltage feedback pin (same as the COMP pin in UC384X),
RI	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency.
SEN	Current sense pin, connect to sense the MOSFET current.
VDD	Supply voltage pin.
GATE	Totem output to drive the external Power MOSFET.

Block Diagram



Simplified Internal Circuit Architecture

Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
V_{DD}	Supply voltage Pin Voltage		40	V
I_{OVP}	VDD OVP maximal enter current		20	mA
V_{FB}	Input Voltage to FB Pin		-0.3 to 6V	V
V_{SEN}	Input Voltage to SEN Pin		-0.3 to 6V	V
P_D	Power Dissipation		300	mW
ESD	ESD Capability, HBM Model		2500	V
	ESD Capability, Machine Model		250	V
T_L	Lead Temperature (Soldering)	20second SOT-23-6L	220	℃
		10second DIP-8	260	℃
T_{STG}	Storage Temperature Range		-55 to + 150	℃

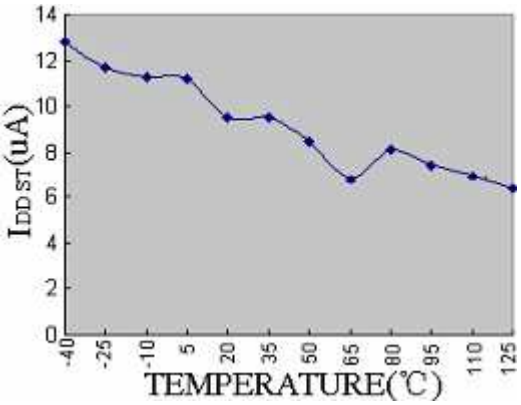
RECOMMENDED OPERATION CONDITION

Symbol	Parameter	Min ~ Max	Unit
VDD	VDD Supply Voltage	11~20	V
RI	RI PIN Resistor Value	65~130	K ohm
T_{OA}	Operation Ambient Temperature	-20~85	℃
P_O	Output Power	0~60	W
F_{PWM}	Frequency of PWM	50~100	kHz

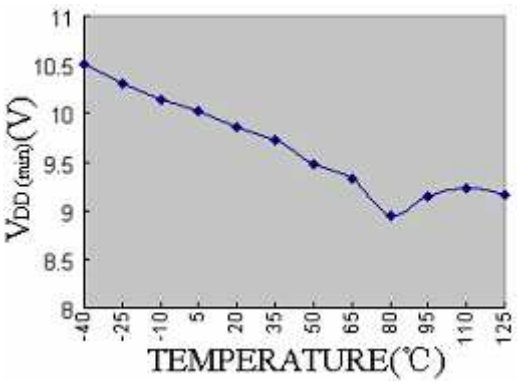
Electrical Characteristics (Ta=25°C unless otherwise noted, V_{DD} = 15V.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD} Pin)						
I_{ST}	Startup Current			8		μA
I_{SS}	Operating Current	V_{FB}=0V		2.9		mA
		V_{FB}=3V		1.9		mA
		V_{FB}=Open		1.44		mA
VDD_{ON}	Turn-on Threshold Voltage			15.3		V
VDD_{OFF}	Turn-off Threshold Voltage			9.8		V
VD_{CLAMP}	VDD Clamp Voltage	I_{VDD}=20mA		25.5		V
Voltage Feedback (FB Pin)						
I_{FB}	Short Circuit Current	V_{FB}=0V		1.68		mA
V_{FB}	Open Loop Voltage	V_{FB}=Open		4.7		V
I_{PFM}	Enter PFM&PWM, FB current			1.2		mA
I_{CRM}	Enter CRM, FB current			1.5		mA
V_{PFM}	PFM Threshold V_{FB}			1.15		V
Current Sensing (SEN Pin)						
V_{TH_L}	Minimum Voltage Lever		0.55	0.65	0.75	V
V_{TH_H}	Maximum Voltage Lever		0.75	0.85	0.95	V
T_{PD}	Delay to Output			300		ns
R_{CS}	Input Impedance			50		KΩ
Oscillator (RI Pin)						
F_{OSC}	Normal Frequency	RI=100Kohm	60	65	70	KHz
F_{PFM}	PFM Frequency	RI=100Kohm		13		KHZ
DC_{MAX}	Maximum Duty Cycle	RI=100Kohm		77		%
ΔF_{TEMP}	Frequency Temp. Stability	-30-85℃		5		%
T_{BLANK}	Leading-Edge Blanking Time			300		nS
GATE Drive Output (GATE Pin)						
V_{OL}	Output Low Level	V_{DD}=15V, I_O=20mA			1	V
V_{OH}	Output High Level	V_{DD}=15V, I_O=20mA	8			V
T_R	Rising Time	C_L=1000pF		420		ns
T_F	Falling Time	C_L=1000pF		120		ns
VG_{CLAMP}	Output Clamp Voltage	VDD=20V		16.8	17.8	V

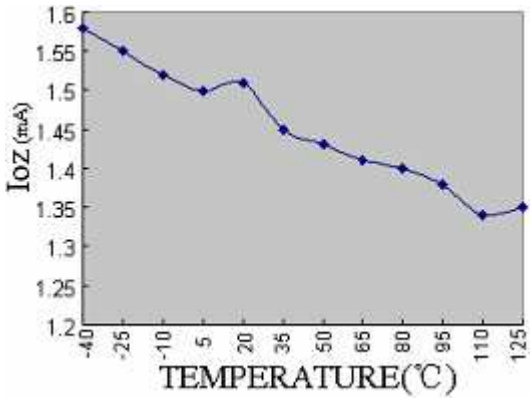
TYPICAL CHARACTERISTICS



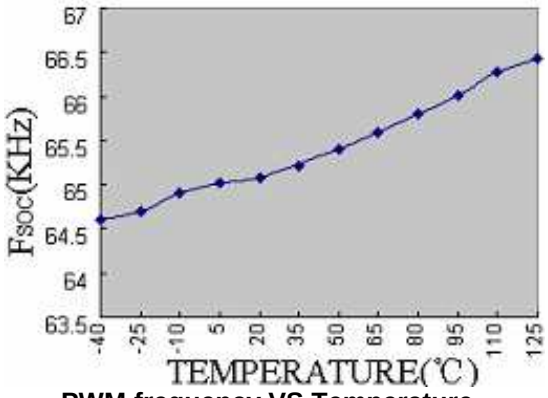
VDD startup Current VS Temperature



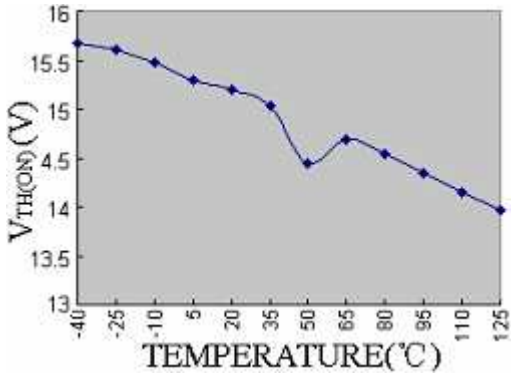
VDD (OFF) VS Temperature



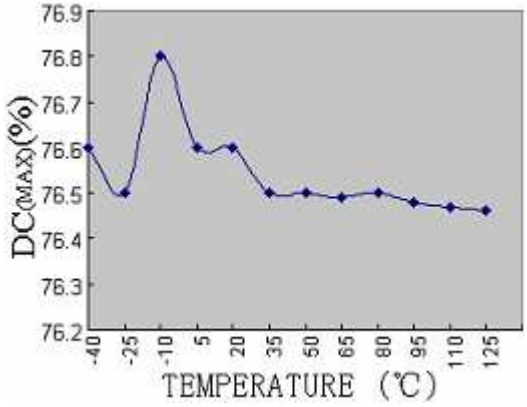
VDD Operation Current VS Temperature



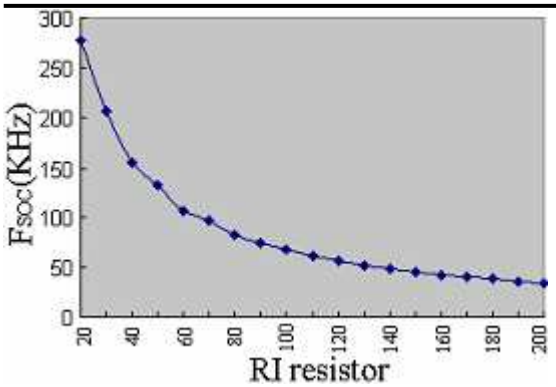
PWM frequency VS Temperature



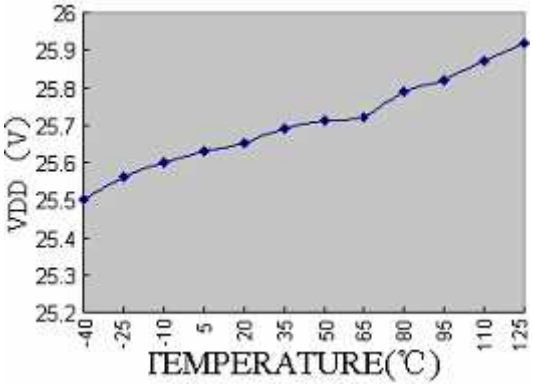
VDD (ON) VS Temperature



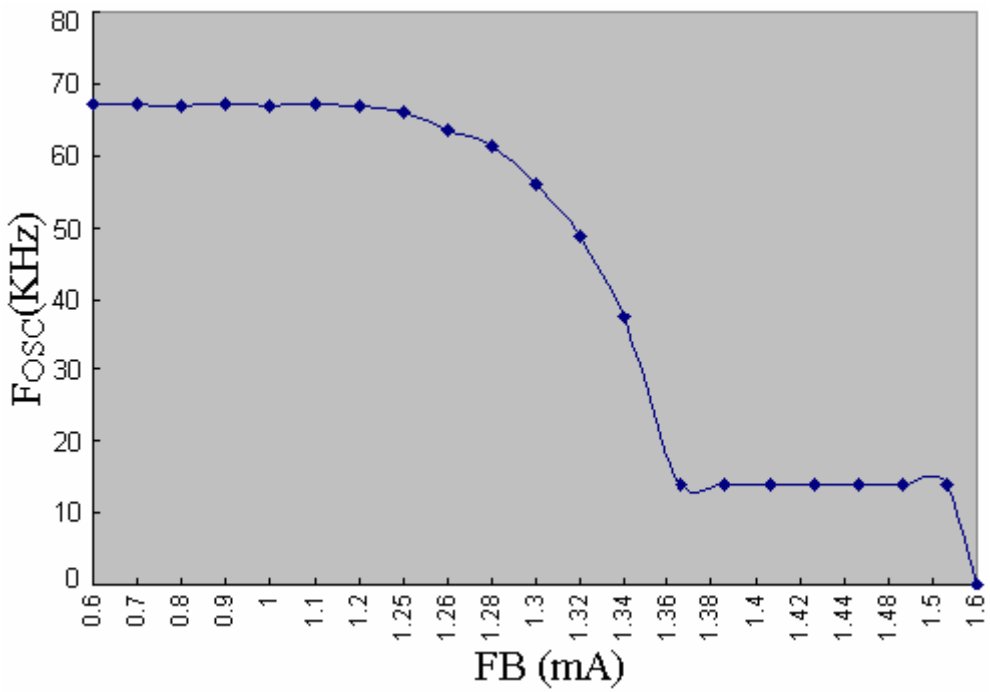
Duty cycle VS Temperature



F_{OSC} VS RI Resistor



OVP VS Temperature



F_{OSC} VS FB Current

OPERATION DESCRIPTION

Current Model

Compared to voltage model control, current model control has a current feedback loop. When the voltage of the sense resistor peak current of the primary winding reaches the internal setting value V_{TH}, comparator reverse, register reset and power MOSFET cut-off. So that to detect and modulate the peak current cycle by cycle could control the output of the power supply. The current feedback has a good linear modulation rate and a fast input and output dynamic impact avoid the pole that the output filter inductance brings and the second class system descends to first class and so it widens the frequency range and optimizes overload protection and short circuit protection.

Startup Current and Under Voltage Lockout

The startup current of CR6850D is set to be very low so that a large value startup resistor can therefore be used to minimize the power loss. For AC to DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor and a 10uF/25V VDD hold capacitor could be used.

The turn-on and turn-off threshold of the CR6850D is designed to 15.3V/9.8V. During startup, the hold-up capacitor must be charge to 15.3V through the startup resistor. The hysteresis is implemented to prevent the shutdown from the voltage dip during startup.

Internal Bias and OSC Operation

A resistor connected between RI pin and GND pin set the internal constant current source to charge or discharge the internal fixed cap. The charge time and discharge time determine the internal clock speed and the switching frequency. Increasing the resistance will reduce the value of the input current and reduce the switching frequency. The relationship between RI pin and PWM switching frequency follows the below equation within the RI allowed range.

$$F_{OSC} = \frac{6500}{RI(K\Omega)}(kHz)$$

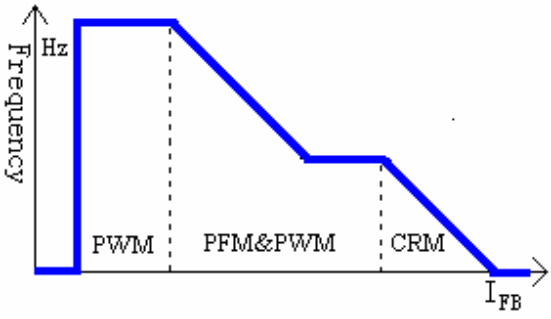
For example, a 100kΩ resistor RI could generate a 50uA constant current and a 65kHz PWM switching frequency. The suggested operating frequency range of CR6850D is within 50KHz to 100KHz.

Green Power Operation

The power dissipation of switching mode power supply is very important in zero load or light load condition. The major dissipation result from conduction loss、switching loss and consume of the control circuit. However, all of them related to the switching frequency. There are many difference topologies has been implemented in different chip. The basic operation theory of all these approaches intended to reduce the switching frequency under light-load or no-load condition.

CR6850D`s green power function adapts PWM、PFM and CRM combining

modulation. When RI resistor is 100k, the PWM frequency is 65kHz in medium or heavy load operation. Through modifying the pulse width, CR6850D could control output voltage. The current of FB pin increases when the load is in light condition and the internal mode controller enters PFM&PWM when the feedback current is over 1.2mA. The operation frequency of oscillator is to descend gradually. The invariable frequency of oscillator is 13kHz when the feedback current is over 1.35mA. To decrease the standby consumption of the power supply , Chip-Rail introduces the Cycle Reset Mode technology；If the feedback current were over 1.5mA, mode controller of CR6850D would reset internal register all the time and cut off the gate pin, while the output voltage is lower than the set value, it would set register, gate pin operating again. Although the frequency of the internal OSC is invariable, the register would reset some pulses so that the practical frequency is decreased at the gate pin.

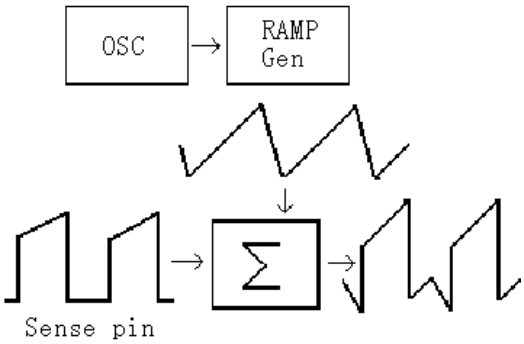


CR6850D Green-Power Function

Internal Synchronized Slop Compensation

Although there are more advantages of the current mode control than conventional voltage mode control, there are still several drawbacks of peak-sensing current-mode converter. Especially the open loop instability when it operates in higher than 50% of the duty-cycle. CR6850D is introduced an internal slope compensation adding voltage ramp to the current sense input voltage for PWM generation to solve this problem. It improves the close loop stability greatly at CCM, prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

$$V_{SLOP} = 0.33 \times \frac{DUTY}{DUTY_{MAX}} = 0.4389 \times DUTY$$



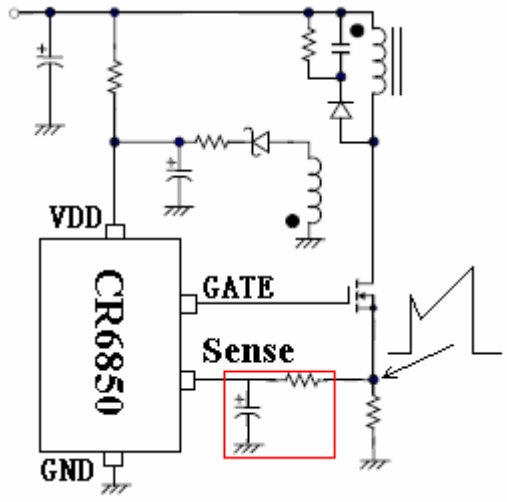
Current Sensing & Dynamic peak limiting

The current flowing by the power MOSFET comes in to being a voltage V_{SENSE} on the sense pin cycle by cycle, which compares to the internal reference voltage, controls the reverse of the internal register, limits the peak current IMAX of the primary of the transformer. The energy $E = \frac{1}{2} \times L \times I_{MAX}^{2}$ deposited by the transformer. So adjusting the R_{SENSE} can set the Max output power of the power supple mode. The current flowing by the

power MOSFET has an extra value $\Delta I = \frac{V_{IN}}{L_P} \times T_D$ due to the system delay T that the current detected from the sense pin to power MOSFET cut off in the CR6850D (Among these, V_{IN} is the primary winding voltage of the transformer and L_P is the primary wind inductance. V_{IN} ranges from 85VAC to 264VAC. To guarantee the output power is a constant for universal input AC voltage, there is a dynamic peak limit circuit to compensate the system delay T that the system delay brings on.

Leading-edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense pin, which would disturb the internal signal from the sampling of the R_{SENSE}. There is a 300n sec leading edge blanking time built in to avoid the effect of the turn-on spike and the power MOSFET cannot be switched off during this time. So that the conventional external RC filtering on sense input is no longer required.



Over Voltage Protection (OVP)

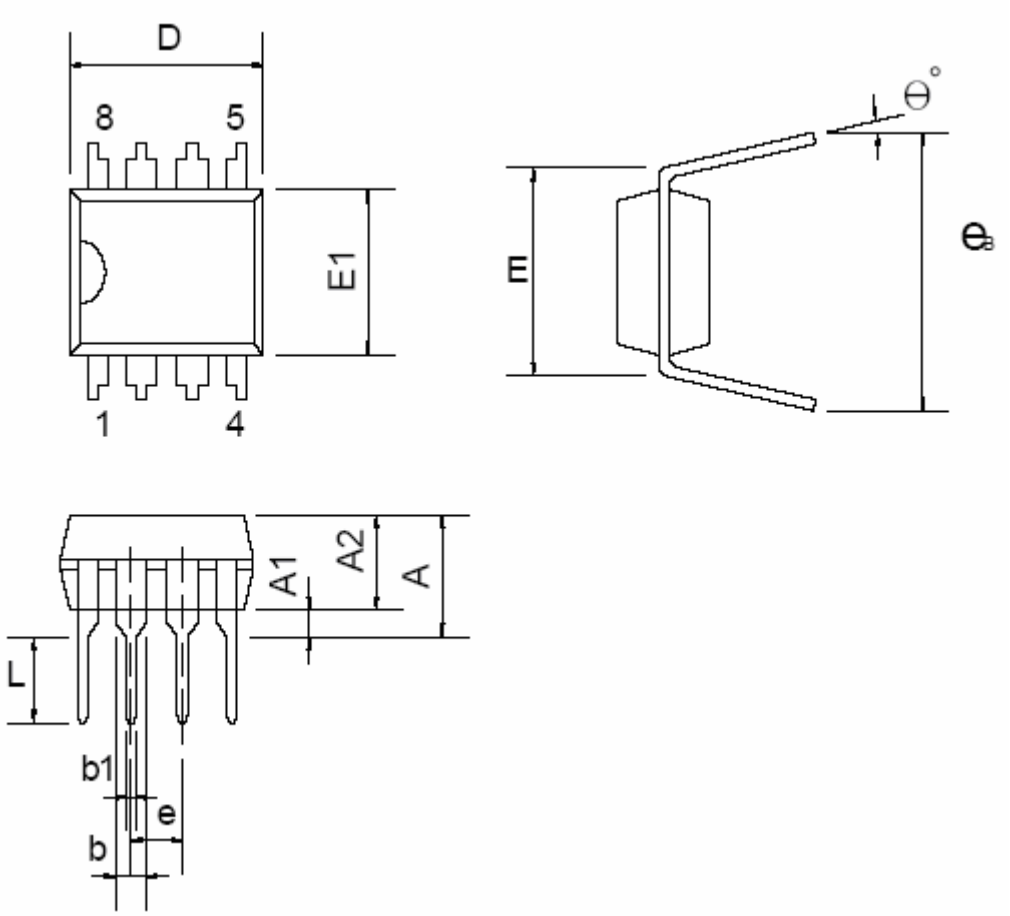
There is a 25.5V over-voltage protection circuit in the CR6850D to improve the credibility and extend the life of the chip. The GATE is to shutdown immediately when the voltage of the VDD is over 25.5V and the voltage of VDD is to descend rapidly.

Gate Driver & Soft Clamped

CR6850D' output designs a totem pole to drive a periphery power MOSFET. The dead time is introduced to minimize the transfixion current when the output is drove. The NMOS is shut off when the other NMOS is turned on. The novel soft clamp technology is introduced to protect the periphery power MOSFET from breaking down and current saturation of the Zener.

PACKAGE DEMENSIONS

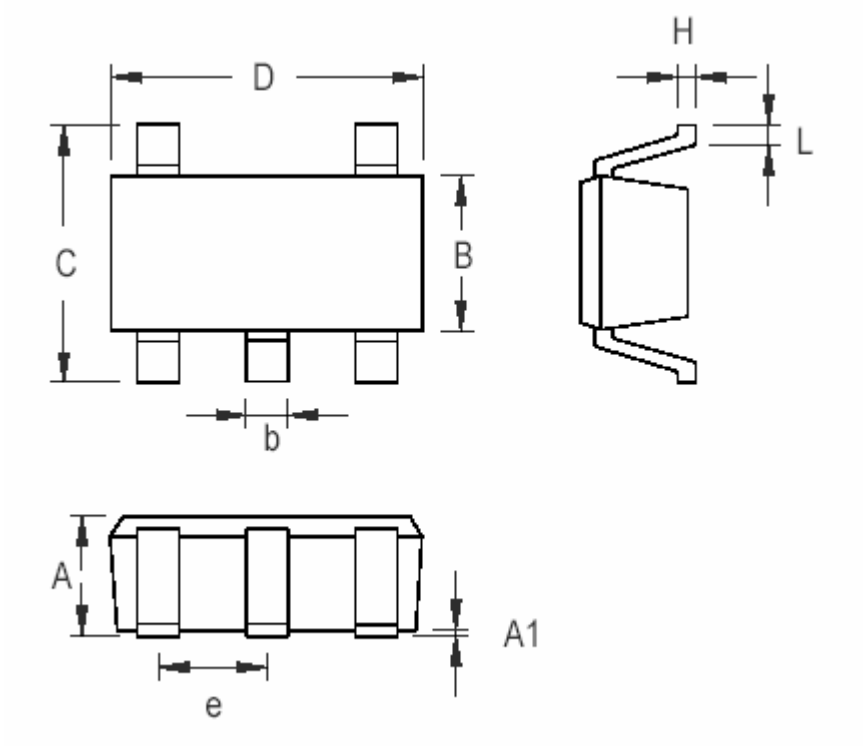
DIP-8L



Dimensions

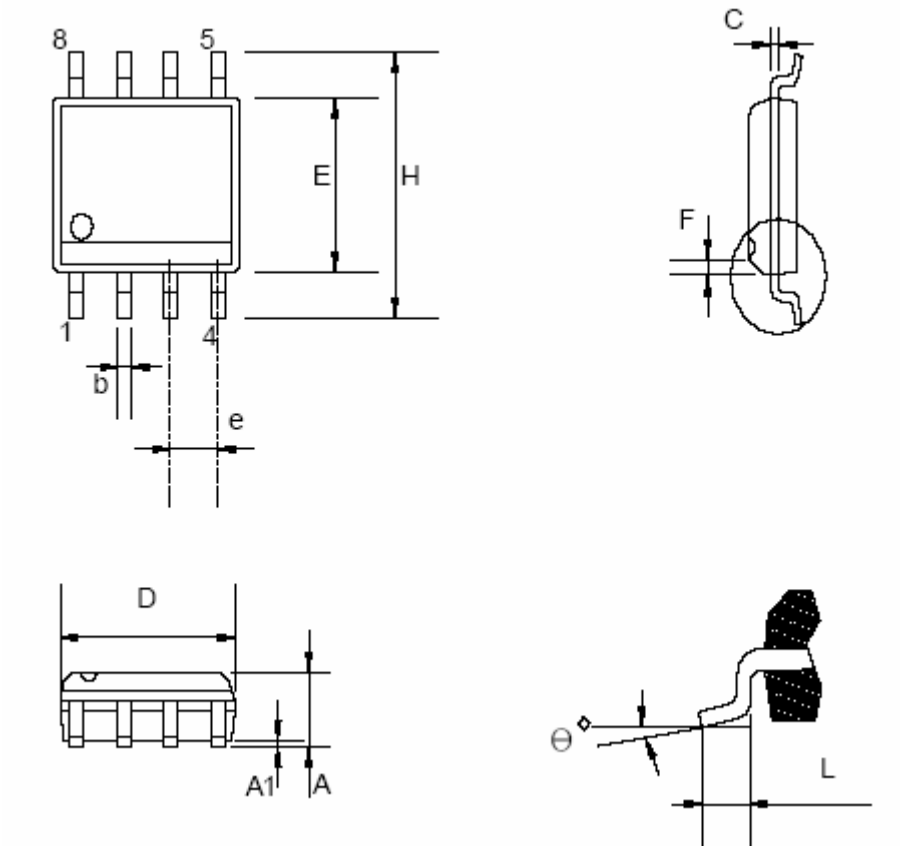
Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

SOT-23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOP-8L



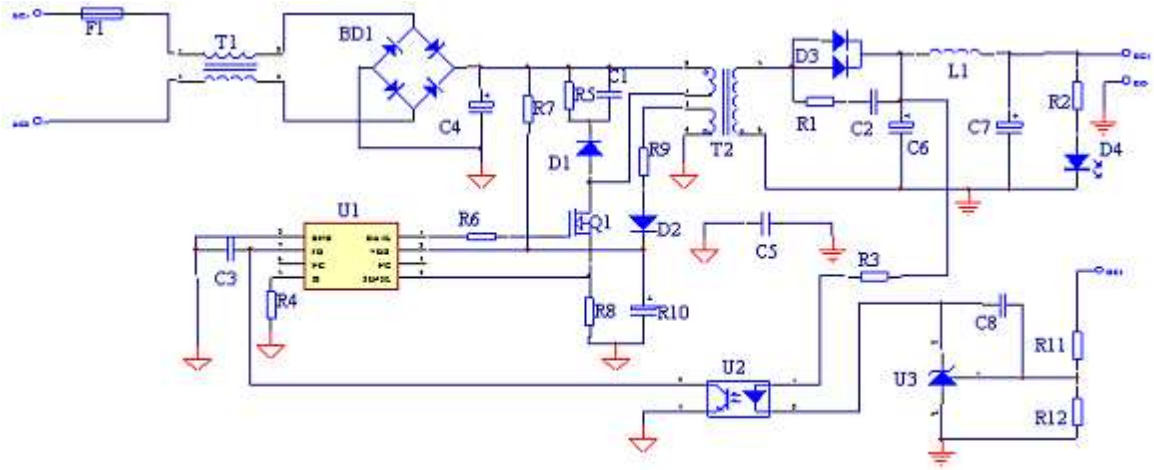
Dimensions DISCLAIMERS

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

REFERENCE CIRCUIT 1

CR6850D drives a periphery Power MOSFET.

5V/6A 30W Power Supply



Quantity	Part Number	Description	Quantity	Part Number	Description
1	C1	102/1000V	1	F1	0.25A
1	C2	103/1000V	1	L1	10uH
1	C3	104	1	R1	20R
1	C4	33uF/400V	2	R2、R3	1K
1	C5	223/1000V	1	R4	100K
1	C7	103/1000V	1	R5	100K/0.5W
1	C8	102/100V	1	R6	47R
2	C6、C7	1000 uF/25V	1	R7	1.5M
1	C8	104	1	R8	0R51
1	BD1	KBL406	1	R9	20R
1	D1	FR107	2	R11、R12	3.3K
1	D2	1N4007	1	U1	CR6850D
1	D3	Y2010D	1	U2	PC817
1	D4	LED	1	U3	TL431
1	T1	20mH	1	Q1	2N60
1	T2	EI-22			

Notice: Q1 is a Power MOSFET