Agilent Technologies

High CMR, High Speed TTL Compatible Optocouplers

Technical Data

6N137
HCNW137 **HCPL-0631**
HCNW2601 **HCPL-0661**
HCNW2611 **HCPL-2601**
HCPL-0600 **HCPL-2611**
HCPL-0601 **HCPL-2630**
HCPL-0611 **HCPL-2631**
HCPL-0630 **HCPL-4661**

Features

- **5 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 50 V for HCPL-X601/X631, HCNW2601 and 10 kV/μs Minimum CMR at V_{CM} = 1000 V for HCPL-X611/X661, HCNW2611**
- **High Speed:** 10 MBd Typical
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature:** -40°C to +85°C
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Strobable Output (Single Channel Products Only)**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute and 5000 V rms* for 1 minute per UL1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak for HCPL-2611 Option 060 and V_{IORM} = 1414 V peak for HCNW137/26X1
- **MIL-STD-1772 Version Available (HCPL-56XX/66XX)**

Applications

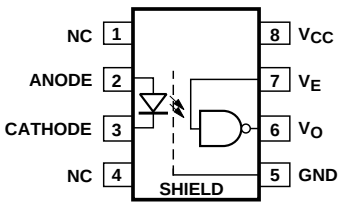
- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**
- **Isolation of High Speed Logic Systems**

Description

The 6N137, HCPL-26XX/06XX/4661, HCNW137/26X1 are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is

Functional Diagram

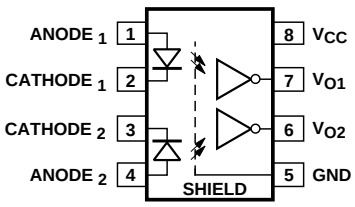
6N137, HCPL-2601/2611
HCPL-0600/0601/0611



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

HCPL-2630/2631/4661
HCPL-0630/0631/0661



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

*5000 V rms/1 Minute rating is for HCNW137/26X1 and Option 020 (6N137, HCPL-2601/11/30/31, HCPL-4661) products only.

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5,000 V/µs for the HCPL-X601/X631 and HCNW2601, and 10,000 V/µs for the HCPL-X611/X661 and HCNW2611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C allowing troublefree system performance.

The 6N137, HCPL-26XX, HCPL-06XX, HCPL-4661, HCNW137, and HCNW26X1 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Selection Guide

Minimum CMR		Input On-Current (mA)	Output Enable	8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)			Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
NA	NA	5	YES	6N137		HCPL-0600		HCNW137	
			NO		HCPL-2630		HCPL-0630		
5,000	50		YES	HCPL-2601		HCPL-0601		HCNW2601	
			NO		HCPL-2631		HCPL-0631		
10,000	1,000		YES	HCPL-2611		HCPL-0611		HCNW2611	
			NO		HCPL-4661		HCPL-0661		
1,000	50		YES	HCPL-2602[1]					
3, 500	300		YES	HCPL-2612[1]					
1,000	50	3	YES	HCPL-261A[1]		HCPL-061A[1]			
			NO		HCPL-263A[1]		HCPL-063A[1]		
1,000[2]	1,000		YES	HCPL-261N[1]		HCPL-061N[1]			
			NO		HCPL-263N[1]		HCPL-063N[1]		
1,000	50	12.5	[3]						HCPL-193X[1] HCPL-56XX[1] HCPL-66XX[1]

Notes:
1. Technical data are on separate Agilent publications.
2. 15 kV/µs with V_{CM} = 1 kV can be achieved using Agilent application circuit.
3. Enable is available for single channel products only, except for HCPL-193X devices.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

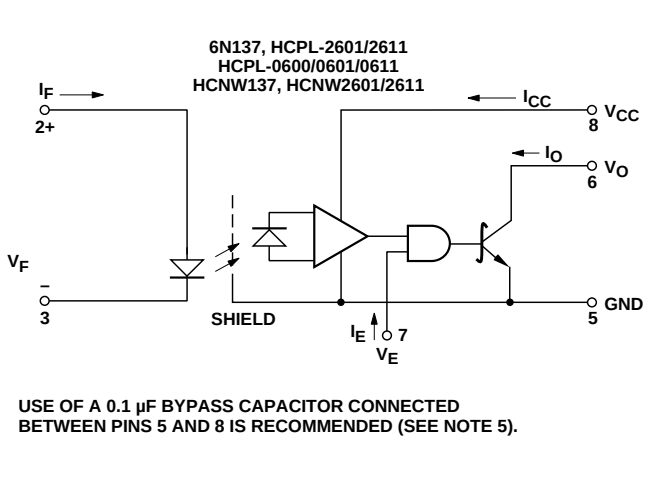
HCPL-2611#XXX

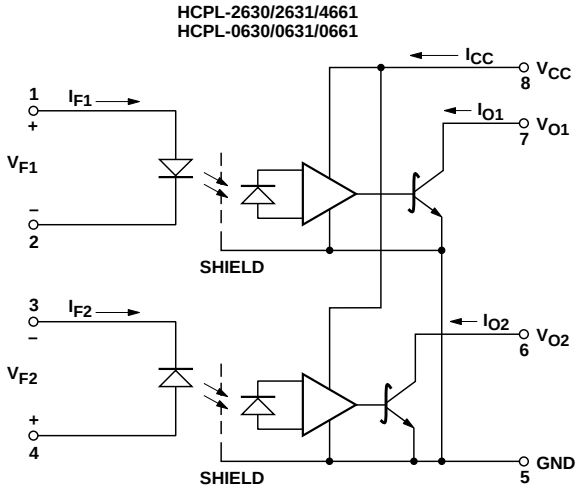
- 020 = 5000 V rms/1 minute UL Rating Option*
- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option**
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact Agilent sales representative or authorized distributor for information.

*For 6N137, HCPL-2601/11/30/31 and HCPL-4661 (8-pin DIP products) only.
**For HCPL-2611 only. Combination of Option 020 and Option 060 is not available.
†Gull wing surface mount option applies to through hole parts only.

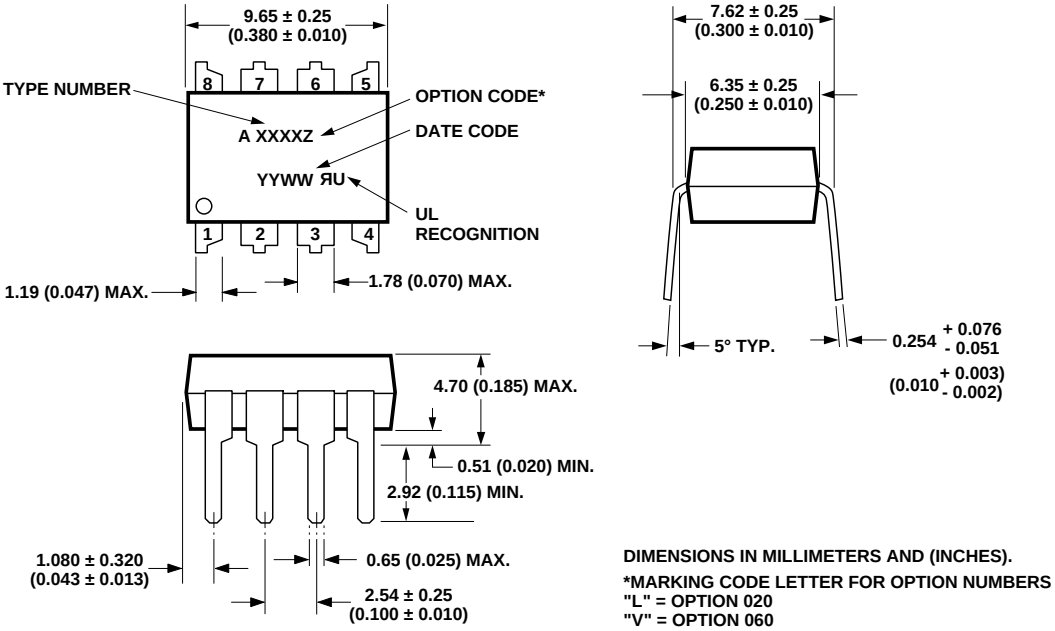
Schematic





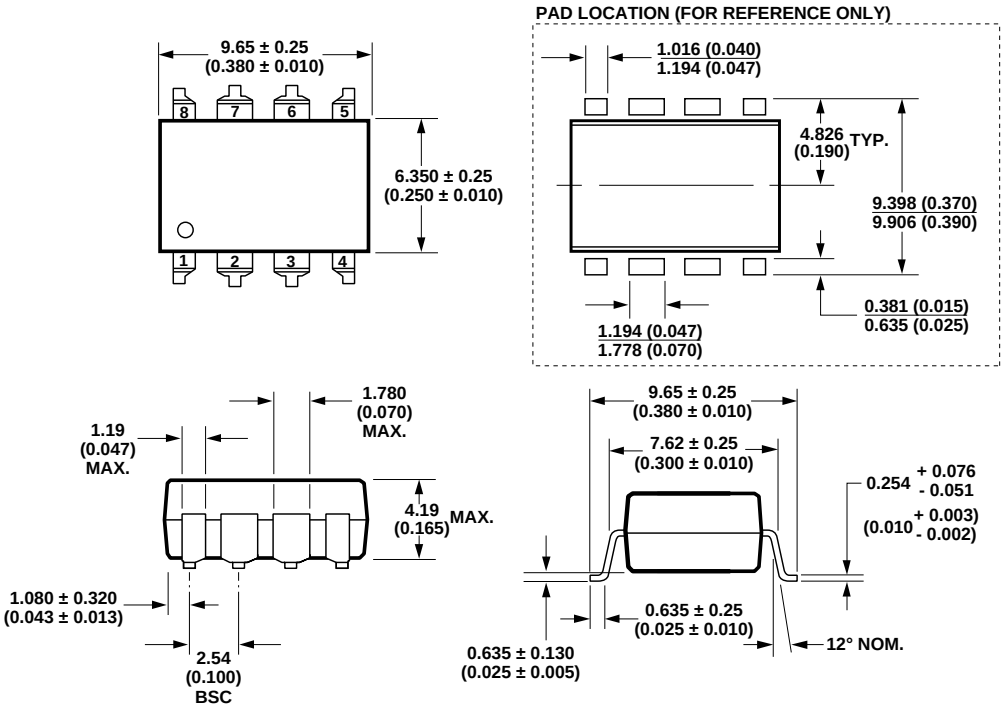
Package Outline Drawings

8-pin DIP Package** (6N137, HCPL-2601/11/30/31, HCPL-4661)

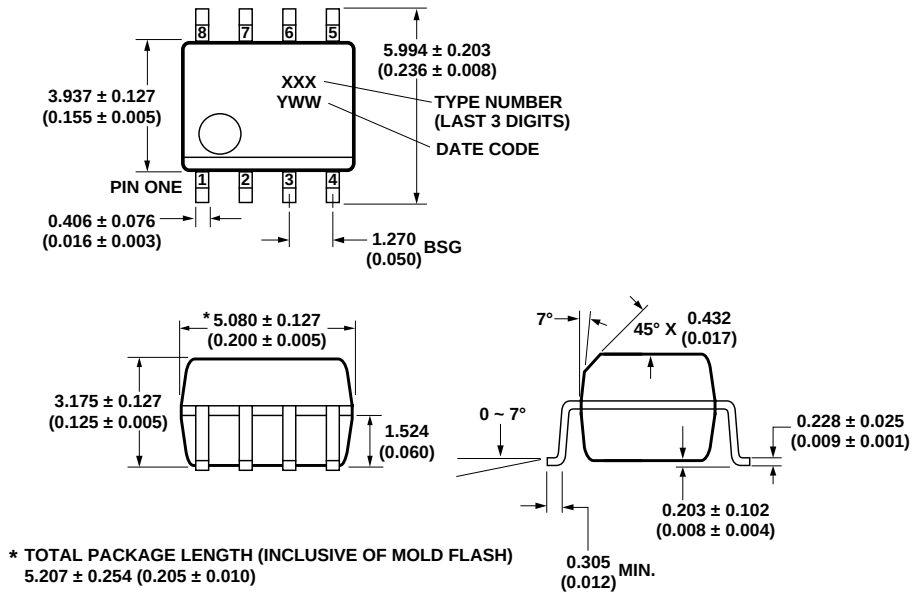


**JEDEC Registered Data (for 6N137 only).

8-pin DIP Package with Gull Wing Surface Mount Option 300 (6N137, HCPL-2601/11/30/31, HCPL-4661)



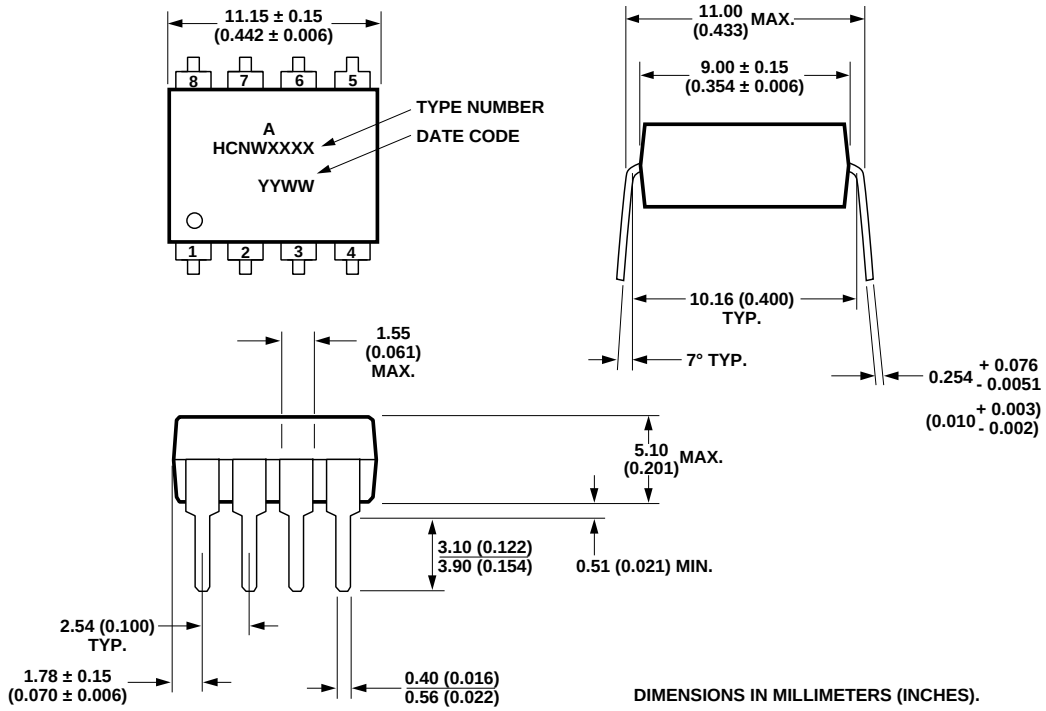
Small-Outline SO-8 Package (HCPL-0600/01/11/30/31/61)



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

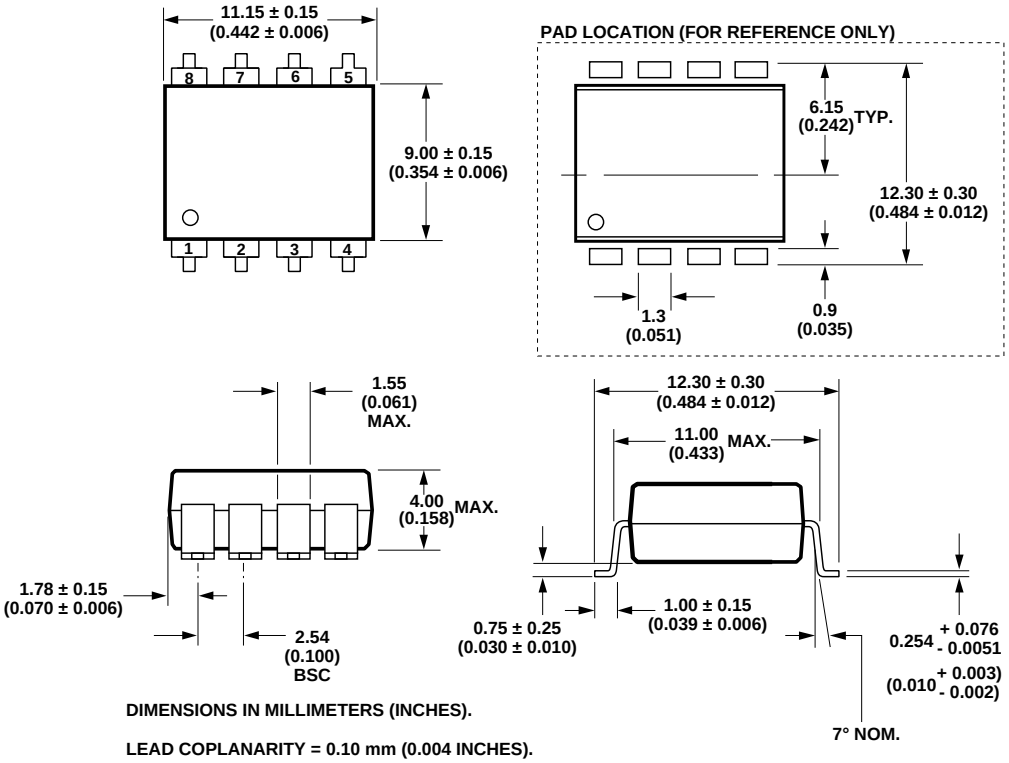
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

8-Pin Widebody DIP Package (HCNW137, HCNW2601/11)

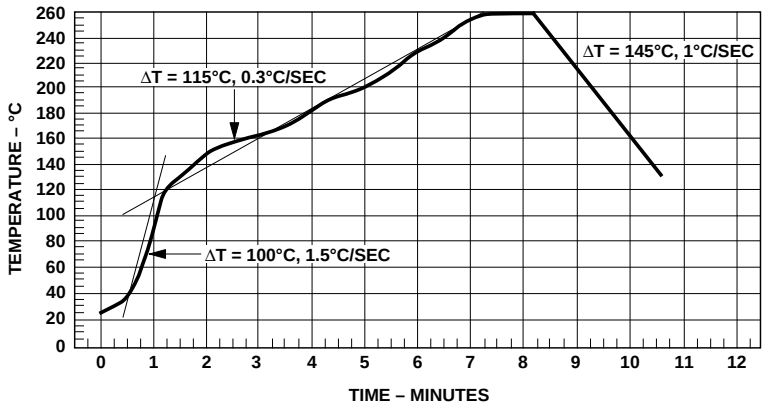


DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW137, HCNW2601/11)



Solder Reflow Temperature Profile (HCPL-06XX and Gull Wing Surface Mount Option 300 Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The 6N137, HCPL-26XX/06XX/46XX, and HCNW137/26XX have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-2611 Option 060 and HCNW137/26X1 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2611 Option 060 Only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

VDE 0884 Insulation Related Characteristics (HCNW137/2601/2611 Only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification (DIN IEC 68 part 1)		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2651	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings* (No Derating Required up to 85°C)

Parameter	Symbol	Package**	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature†	T_A		-40	85	°C	
Average Forward Input Current	I_F	Single 8-Pin DIP Single SO-8 Widebody		20	mA	2
		Dual 8-Pin DIP Dual SO-8		15		1, 3
Reverse Input Voltage	V_R	8-Pin DIP, SO-8		5	V	1
		Widebody		3		
Input Power Dissipation	P_I	Widebody		40	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E	Single 8-Pin DIP Single SO-8 Widebody		V_{CC} + 0.5	V	
Enable Input Current	I_E			5	mA	
Output Collector Current	I_O			50	mA	1
Output Collector Voltage (Selection for Higher Output Voltages up to 20 V is Available.)	V_O			7	V	1
Output Collector Power Dissipation	P_O	Single 8-Pin DIP Single SO-8 Widebody		85	mW	
		Dual 8-Pin DIP Dual SO-8		60		1, 4
Lead Solder Temperature (Through Hole Parts Only)	T_{LS}	8-Pin DIP	260°C for 10 sec., 1.6 mm below seating plane			
		Widebody	260°C for 10 sec., up to seating plane			
Solder Reflow Temperature Profile (Surface Mount Parts Only)		SO-8 and Option 300	See Package Outline Drawings section			

*JEDEC Registered Data (for 6N137 only).
Ratings apply to all devices except otherwise noted in the **Package column.
†0°C to 70°C on JEDEC Registration.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	µA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
Low Level Enable Voltage†	V_{EL}	0	0.8	V
High Level Enable Voltage†	V_{EH}	2.0	V_{CC}	V
Operating Temperature	T_A	-40	85	°C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.
†For single channel products only.

Electrical Specifications

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. All Typicals at V_{CC} = 5 V, T_A = 25°C. All enable test conditions apply to single channel products only. See note 5.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*	All		5.5	100	µA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 5.5 V, I_F = 250 µA	1	1, 6, 19
Input Threshold Current	I_{TH}	Single Channel Widebody		2.0	5.0	mA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2, 3	19
		Dual Channel		2.5					
Low Level Output Voltage	V_{OL}*	8-Pin DIP SO-8		0.35	0.6	V	V_{CC} = 5.5 V, V_E = 2.0 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	2, 3, 4, 5	1, 19
		Widebody		0.4					
High Level Supply Current	I_{CCH}	Single Channel		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 0 mA		7
				6.5			V_E = V_{CC}		
		Dual Channel		10	15		Both Channels		
Low Level Supply Current	I_{CCL}	Single Channel		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 10 mA		8
				8.5			V_E = V_{CC}		
		Dual Channel		13	21		Both Channels		
High Level Enable Current	I_{EH}	Single Channel		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*			-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		9
High Level Enable Voltage	V_{EH}		2.0			V			19
Low Level Enable Voltage	V_{EL}				0.8	V			
Input Forward Voltage	V_F	8-Pin DIP	1.4	1.5	1.75*	V	T_A = 25°C; I_F = 10 mA	6, 7	1
		SO-8	1.3		1.80				
		Widebody	1.25	1.64	1.85		T_A = 25°C		
			1.2		2.05				
Input Reverse Breakdown Voltage	BV_R*	8-Pin DIP SO-8	5			V	I_R = 10 µA		1
		Widebody	3				I_R = 100 µA, T_A = 25°C		
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$	8-Pin DIP SO-8		-1.6		mV/°C	I_F = 10 mA	7	1
		Widebody		-1.9					
Input Capacitance	C_{IN}	8-Pin DIP SO-8		60		pF	f = 1 MHz, V_F = 0 V		1
		Widebody		70					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to +70°C. HP specifies -40°C to +85°C.

Switching Specifications (AC)

Over Recommended Temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 5 V.

Parameter	Sym.	Package**	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75* 100	ns	T_A = 25°C, R_L = 350 Ω, C_L = 15 pF	8, 9, 10	1, 10, 19
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75* 100	ns	T_A = 25°C		1, 11, 19
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	8-Pin DIP SO-8 Widebody		3.5	35 40	ns		8, 9, 10, 11	13, 19
Propagation Delay Skew	t_{PSK}				40	ns			12, 13, 19
Output Rise Time (10-90%)	t_r			24		ns		12	1, 19
Output Fall Time (90-10%)	t_f			10		ns		12	1, 19
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	Single Channel		30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	13, 14	14
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	Single Channel		20		ns			15

*JEDEC registered data for the 6N137.
Ratings apply to all devices except otherwise noted in the **Package column.

Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	6N137 HCPL-2630 HCPL-0600/0630 HCNW137		10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	15	1, 16, 18, 19
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	5,000	10,000		$\|V_{CM}\|$ = 50 V			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	10,000	15,000		$\|V_{CM}\|$ = 1 kV			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	6N137 HCPL-2630 HCPL-0600/0630 HCNW137		10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	15	1, 17, 18, 19
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	5,000	10,000		$\|V_{CM}\|$ = 50 V			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	10,000	15,000		$\|V_{CM}\|$ = 1 kV			

Package Characteristics

All Typicals at T_A = 25°C.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Insulation	I_{I-O}*	Single 8-Pin DIP Single SO-8			1	µA	45% RH, t = 5 s, V_{I-O} = 3 kV dc, T_A = 25°C		20, 21
Input-Output Momentary Withstand Voltage**	V_{ISO}	8-Pin DIP, SO-8	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		20, 21
		Widebody	5000						20, 22
		OPT 020†	5000						
Input-Output Resistance	R_{I-O}	8-Pin DIP, SO-8		10^{12}		Ω	V_{I-O} = 500 V dc		1, 20, 23
		Widebody	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	8-Pin DIP, SO-8		0.6		pF	f = 1 MHz, T_A = 25°C		1, 20, 23
		Widebody		0.5	0.6				
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		µA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 V		24
Resistance (Input-Input)	R_{I-I}	Dual Channel		10^{11}		Ω			24
Capacitance (Input-Input)	C_{I-I}	Dual 8-Pin DIP		0.03		pF	f = 1 MHz		24
		Dual SO-8		0.25					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to 70°C. HP specifies -40°C to 85°C.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or Agilent Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
†For 6N137, HCPL-2601/2611/2630/2631/4661 only.

Notes:

1. Each channel.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
4. Derate linearly above 80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
5. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 17. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
6. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 µA. HP guarantees a maximum I_{OH} of 100 µA.
7. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. HP guarantees a maximum I_{CCH} of 10 mA.
8. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. HP guarantees a maximum I_{CCL} of 13 mA.
9. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of –2.0 mA. HP guarantees a maximum I_{EL} of -1.6 mA.
10. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
11. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
12. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
13. See application section titled "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.
14. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
15. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
16. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
17. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
18. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}(p\text{-}p)$.

19. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only.
20. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
21. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
22. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
23. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.
24. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

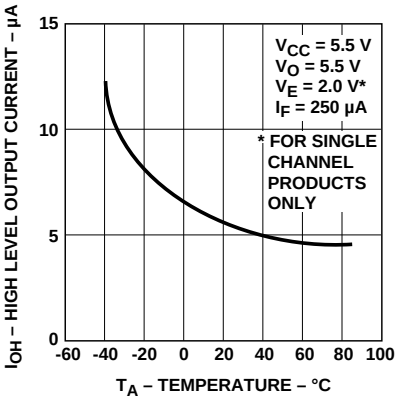


Figure 1. Typical High Level Output Current vs. Temperature.

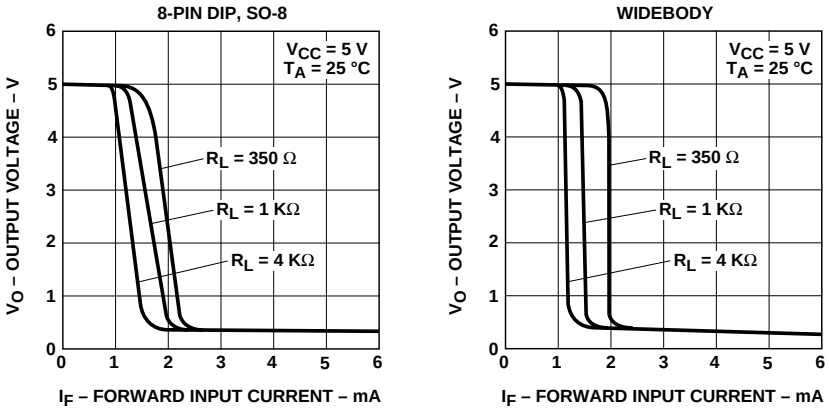


Figure 2. Typical Output Voltage vs. Forward Input Current.

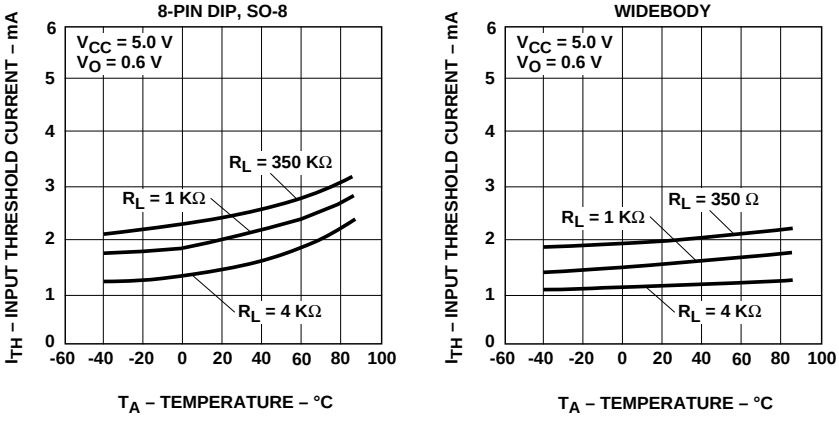
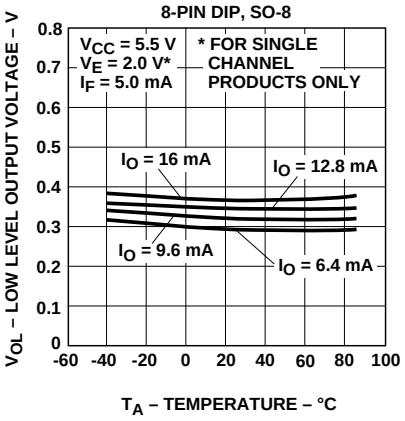


Figure 3. Typical Input Threshold Current vs. Temperature.



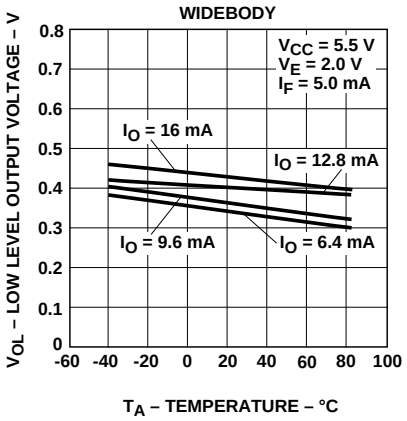


Figure 4. Typical Low Level Output Voltage vs. Temperature.

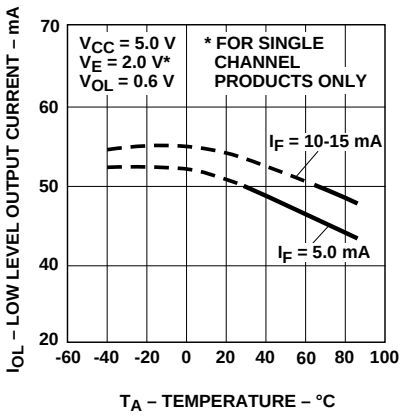
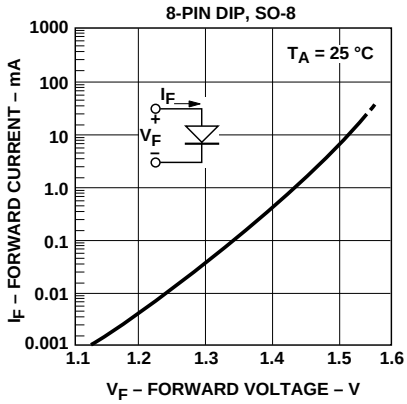


Figure 5. Typical Low Level Output Current vs. Temperature.



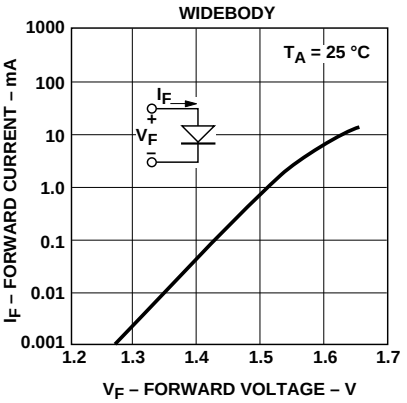
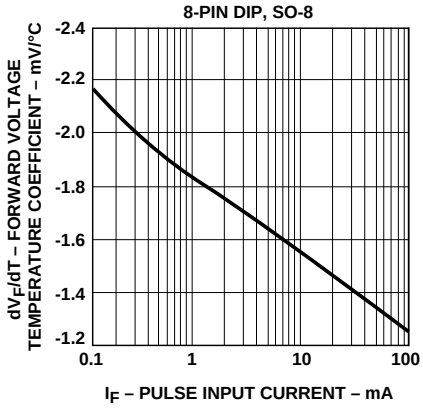


Figure 6. Typical Input Diode Forward Characteristic.



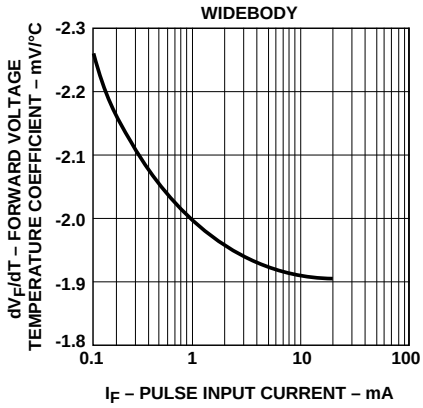


Figure 7. Typical Temperature Coefficient of Forward Voltage vs. Input Current.

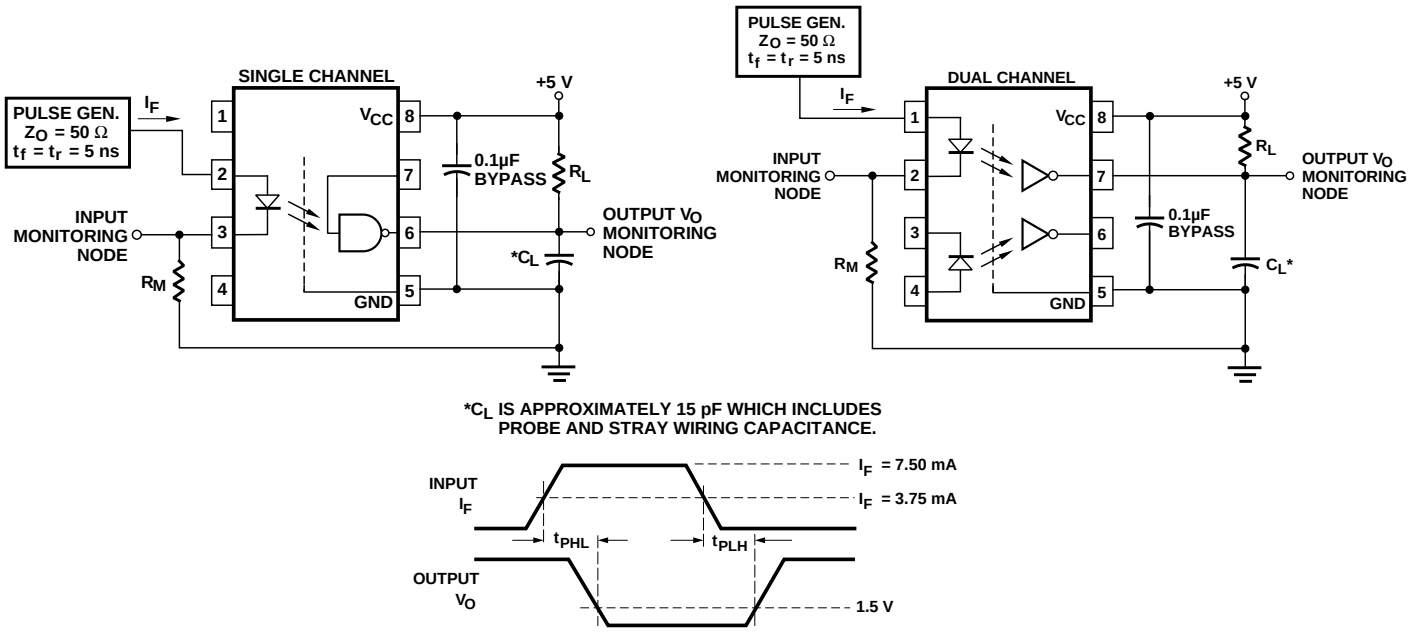


Figure 8. Test Circuit for t_{PHL} and t_{PLH}.

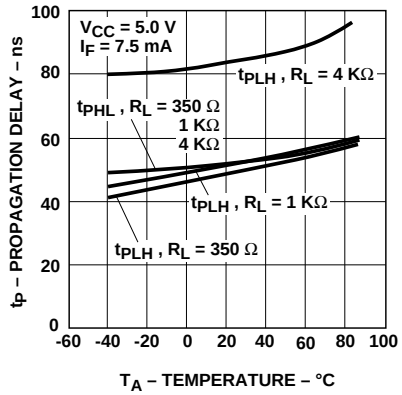


Figure 9. Typical Propagation Delay vs. Temperature.

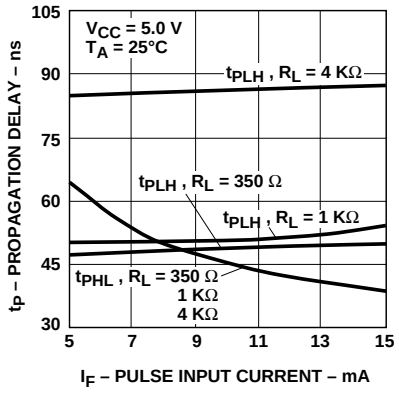


Figure 10. Typical Propagation Delay vs. Pulse Input Current.

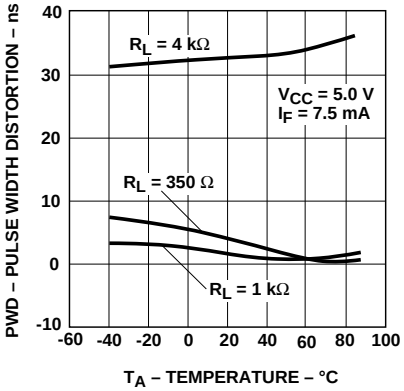


Figure 11. Typical Pulse Width Distortion vs. Temperature.

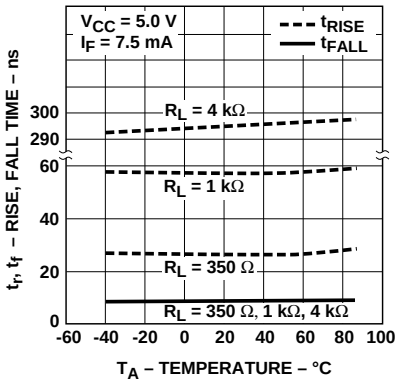


Figure 12. Typical Rise and Fall Time vs. Temperature.

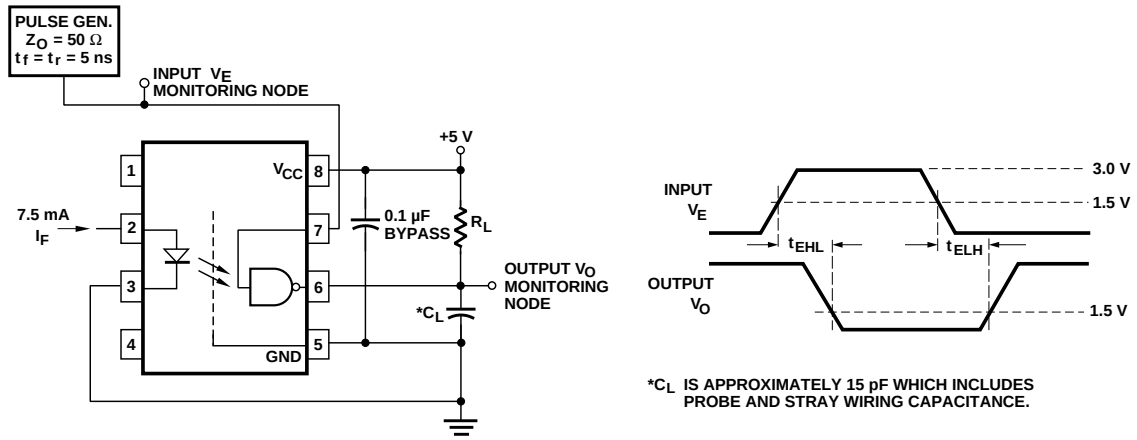


Figure 13. Test Circuit for t_{EHL} and t_{ELH}.

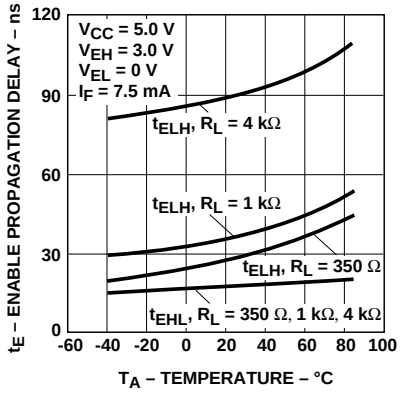


Figure 14. Typical Enable Propagation Delay vs. Temperature.

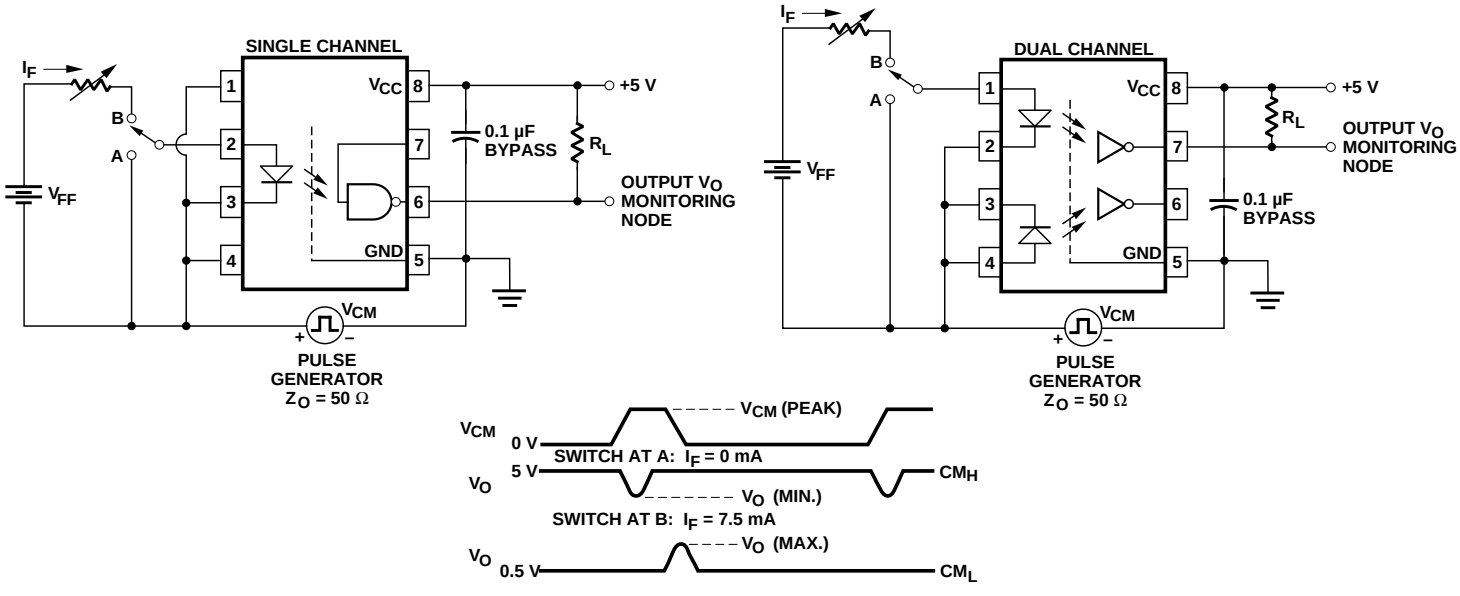


Figure 15. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

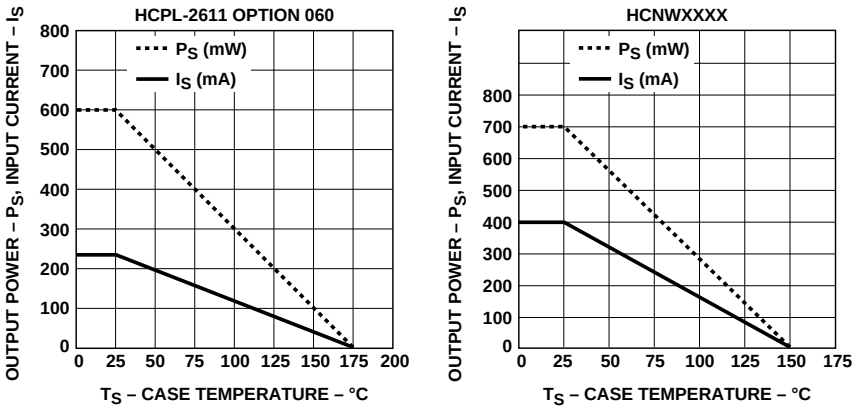


Figure 16. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

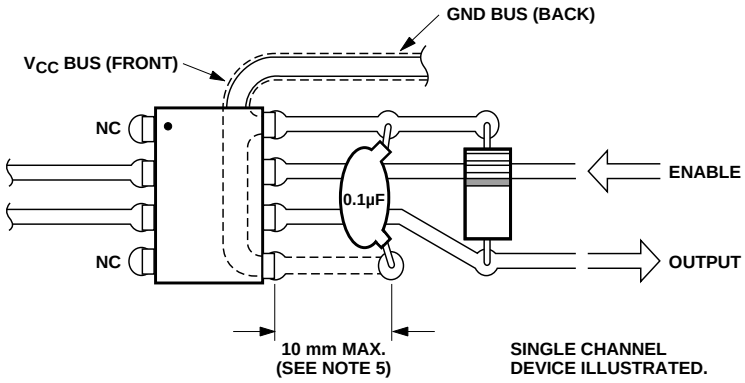
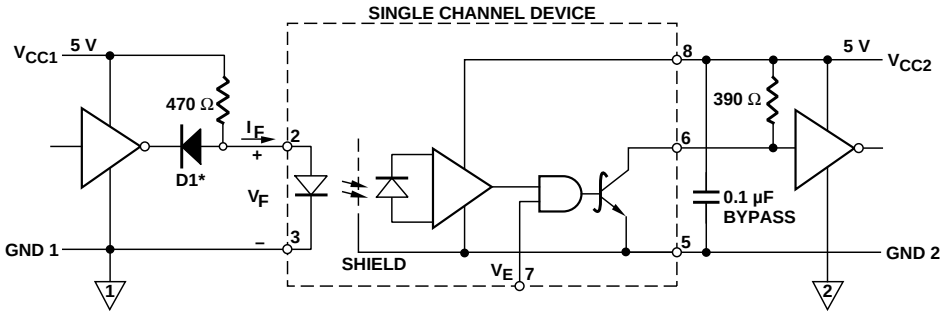


Figure 17. Recommended Printed Circuit Board Layout.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

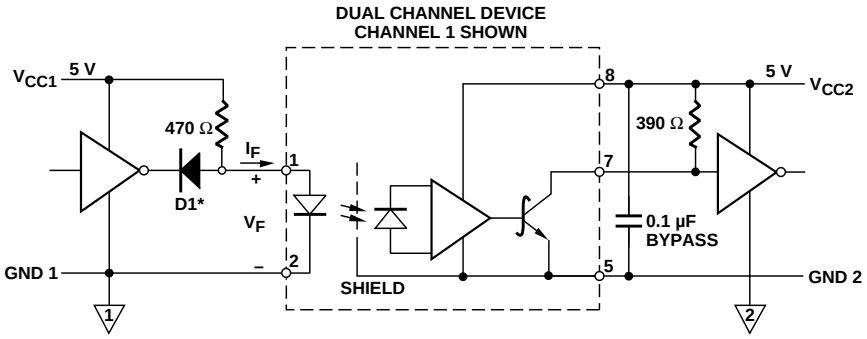


Figure 18. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output causing the output to change from high to low (see Figure 8).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-l, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 19, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 20 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 20 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulsewidth distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

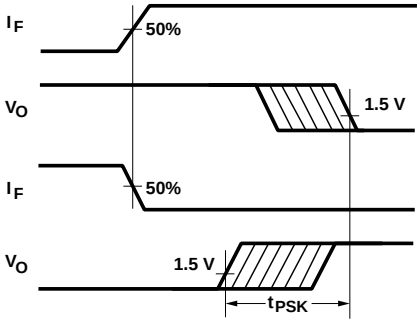


Figure 19. Illustration of Propagation Delay Skew - t_{PSK}.

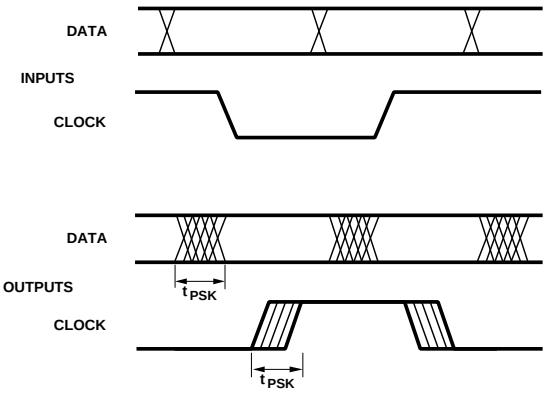


Figure 20. Parallel Data Transmission Example.

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