HEF4015B

Dual 4-bit static shift register

Rev. 06 — 3 November 2009 **Product data sheet**

1. General description

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (Q0 to Q3) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces Q0 to Q3 to LOW, independent of CP and D. The clock input's Schmitt trigger action makes the input highly tolerant of slower clock rise and fall times.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input. It is also suitable for use over the full industrial (−40 °C to +85 °C) temperature range.

2. Features

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the automotive temperature range −40 °C to +85 °C.
- Complies with JEDEC standard JESD 13-B

3. Applications

- Serial-to-parallel converter
- Buffer stores
- General purpose register

4. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +85 °C.

| Type number	Package			Version
	Name	**Description**		
HEF4015BP	DIP16	plastic dual in-line package; 16 leads (300 mil)		SOT38-4
HEF4015BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm		SOT109-1

## 5. Functional diagram
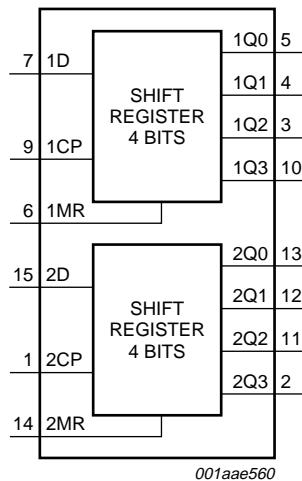
Fig 1.   Functional diagram
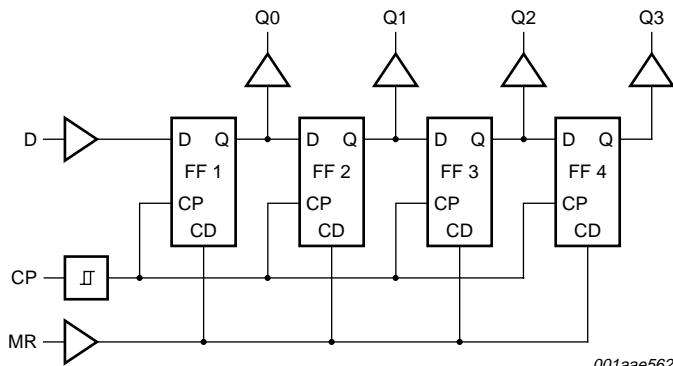
**Fig 2.   Logic diagram for one register**

6. Pinning information

6.1 Pinning

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2CP	1	16	V_{DD}
2Q3	2	15	2D
1Q2	3	14	2MR
1Q1	4	13	2Q0
1Q0	5	12	2Q1
1MR	6	11	2Q2
1D	7	10	1Q3
V_{SS}	8	9	1CP

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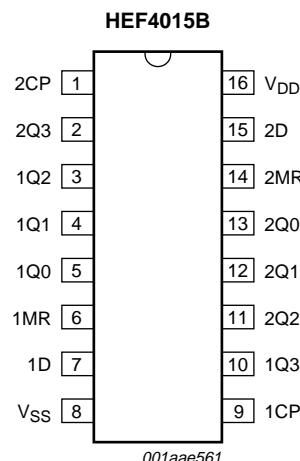
Fig 3.   Pin configuration

6.2 Pin description

Table 2.   Pin description

Symbol	Pin	Description
1Q0 to 1Q3	5, 4, 3, 10	parallel output
2Q0 to 2Q3;	13, 12, 11, 2	parallel output
1MR, 2MR	6, 14	master reset input (active HIGH)
1D, 2D	7, 15	serial data input
V_{SS}	8	ground supply voltage
1CP, 2CP	9, 1	clock input (LOW-to-HIGH edge-triggered)
V_{DD}	16	supply voltage

7. Functional description

Table 3.   Function table [1]

number of clock pulse transitions	Input			Output			
	CP	D	MR	Q0	Q1	Q2	Q3
1	↑	D1	L	D1	X	X	X
2	↑	D2	L	D2	D1	X	X
3	↑	D3	L	D3	D2	D1	X
4	↑	D4	L	D4	D3	D2	D1
	↓	X	L	no change	no change	no change	no change
	X	X	H	L	L	L	L

[1]   H = HIGH voltage level; L = LOW voltage level; X = don't care; Dn = either HIGH or LOW;
↑ = positive-going transition; ↓ = negative-going transition.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			−0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1]   For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2]   For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	-	3.75	µs/V
		$V_{DD} = 10$ V	-	-	0.5	µs/V
		$V_{DD} = 15$ V	-	-	0.08	µs/V

10. Static characteristics

Table 6.   Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	
V_{IH}	HIGH-level input voltage	$|I_O|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$|I_O|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$|I_O|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$|I_O|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	−1.7	-	−1.4	-	−1.1	-	mA
		V_O = 4.6 V	5 V	−0.52	-	−0.44	-	−0.36	-	mA
		V_O = 9.5 V	10 V	−1.3	-	−1.1	-	−0.9	-	mA
		V_O = 13.5 V	15 V	−3.6	-	−3.0	-	−2.4	-	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

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11. Dynamic characteristics

Table 7. Dynamic characteristics
$V_{SS} = 0$ V; $C_L = 50$ pF; $T_{amb} = 25\,°C$.

| Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nCP to Qn; see Figure 4	5 V	103 ns + (0.55 ns/pF)C_L	-	130	260	ns
			10 V	44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns
		nMR to Qn; see Figure 6	5 V	78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V	34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V	27 ns + (0.16 ns/pF)C_L	-	35	70	ns
t_{PLH}	LOW to HIGH propagation delay	nCP to Qn see Figure 4	5 V	93 ns + (0.55 ns/pF)C_L	-	120	240	ns
			10 V	44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns
t_t	transition time	see Figure 4	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{su}	set-up time	nD to nCP; see Figure 5	5 V		+25	−15	-	ns
			10 V		+25	−10	-	ns
			15 V		+20	−5	-	ns
t_h	hold time	nD to nCP; see Figure 5	5 V		40	20	-	ns
			10 V		20	10	-	ns
			15 V		15	8	-	ns
t_W	pulse width	nCP LOW; minimum width; see Figure 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nMR HIGH; minimum width; see Figure 6	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
t_{rec}	recovery time	pin nMR; see Figure 6	5 V		50	20	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
f_{max}	maximum frequency	see Figure 5	5 V		7	15	-	MHz
			10 V		15	30	-	MHz
			15 V		22	44	-	MHz
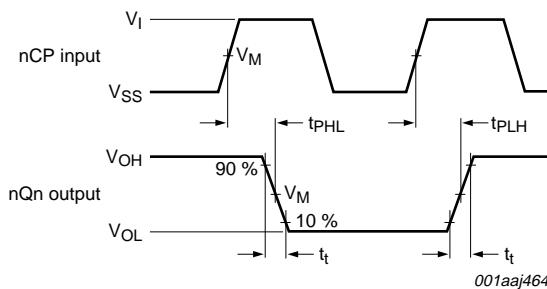
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8.   Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.
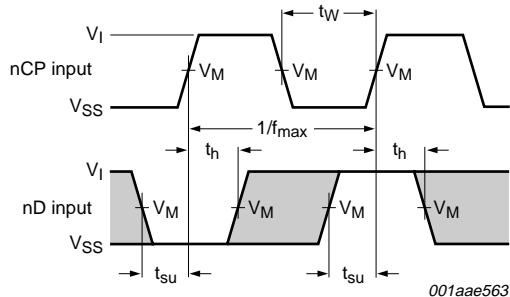
Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 6300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 17000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

12. Waveforms

Measurement points are given in Table 9.

**Fig 4.   Waveforms showing nCP propagation delays and nQn transition times**
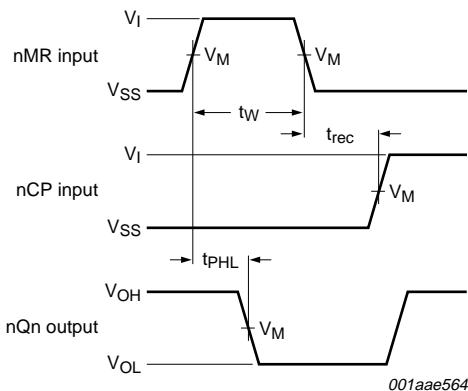
The shaded area indicates where the input is permitted to change for predictable output performance.

Set-up and hold times are shown as positive values but may be specified as negative values;

Measurement points are given in Table 9.

**Fig 5.   Waveforms showing set-up times, hold times, and minimum clock pulse width**
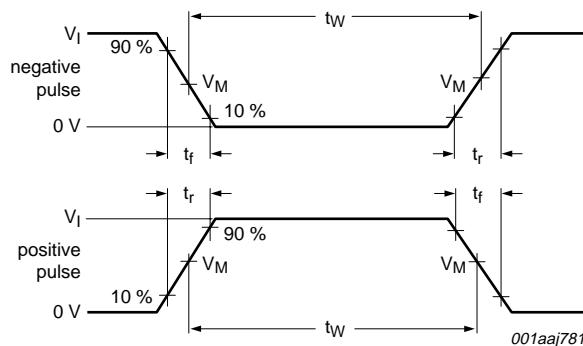
Measurement points are given in Table 9.
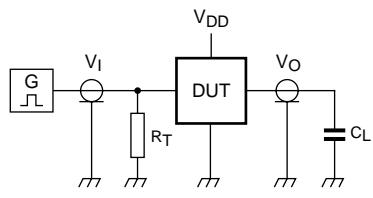
Fig 6. **Waveforms showing MR recovery time, propagation delay and minimum pulse width**

Table 9. **Measurement points**

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$

a. Input waveforms

b. Test circuit

Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 7. Test circuit for measuring switching times
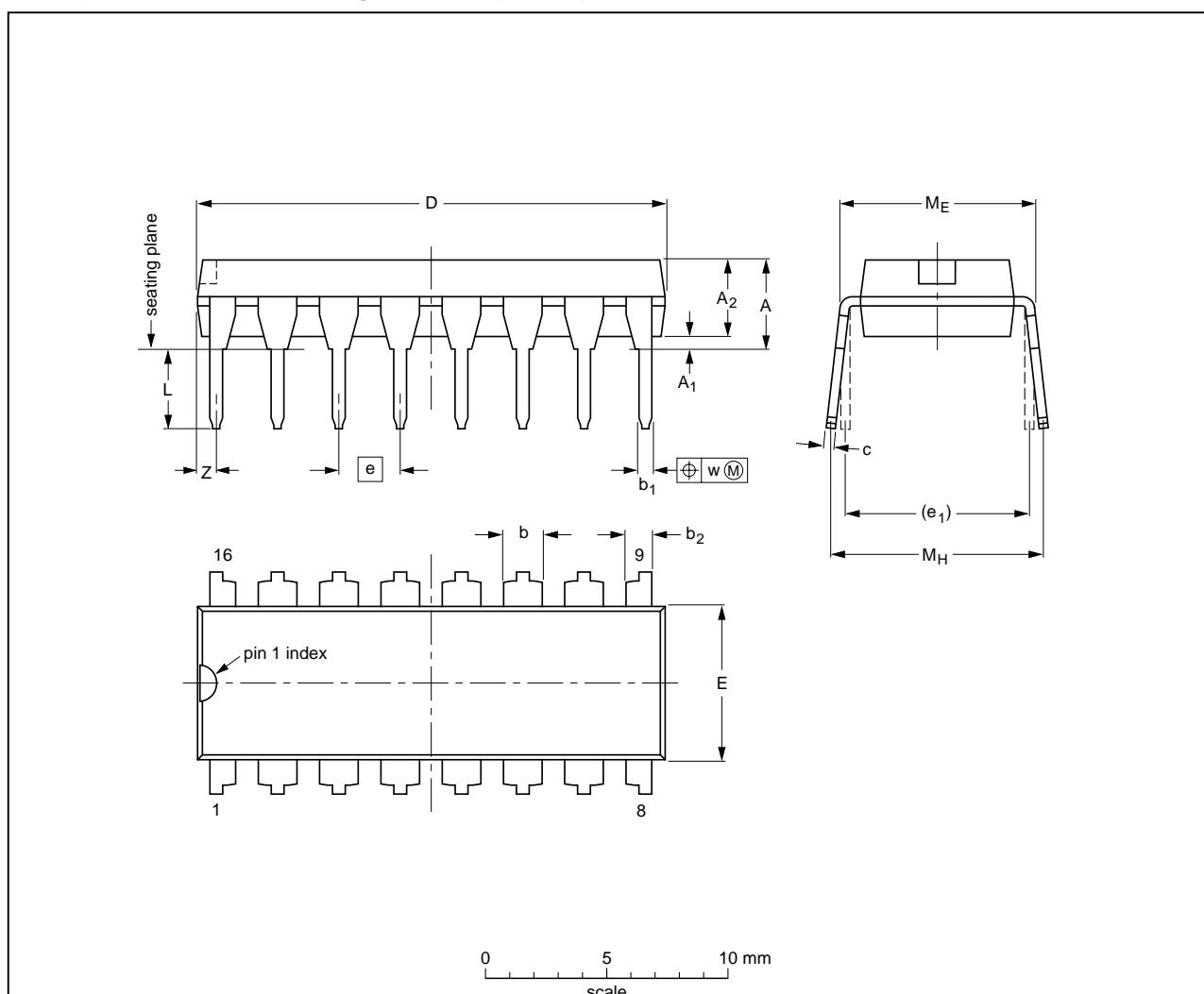
Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	$\leq$ 20 ns	50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	b₂	c	D[1]	E[1]	e	e₁	L	M_E	M_H	w	Z[1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 8.   Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D[1]	E[1]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 9.   Package outline SOT109-1 (SO16)

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14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4015B_6	20091103	Product data sheet	-	HEF4015B_5
Modifications:	• Section 9 "Recommended operating conditions", $\Delta t/\Delta V$ values updated.			
HEF4015B_5	20090624	Product data sheet	-	HEF4015B_4
HEF4015B_4	20090127	Product data sheet	-	HEF4015B_CNV_3
HEF4015B_CNV_3	19950101	Product specification	-	HEF4015B_CNV_2
HEF4015B_CNV_2	19950101	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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