

IRF7342

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual P-Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

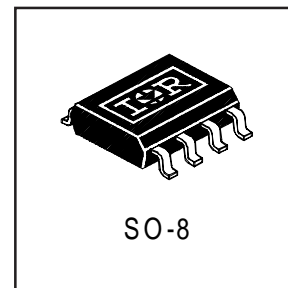
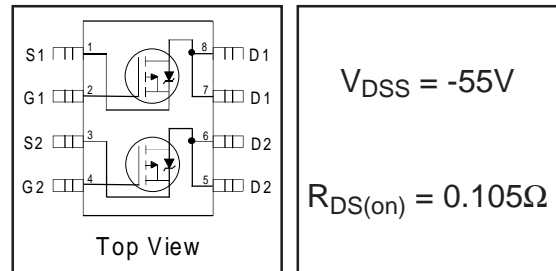
The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	-55	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	-3.4	A
$I_D @ T_C = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	-2.7	
I_{DM}	Pulsed Drain Current ①	-27	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	2.0	W
$P_D @ T_C = 70^\circ\text{C}$	Power Dissipation	1.3	
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
V_{GSM}	Gate-to-Source Voltage Single Pulse $t_p < 10\mu\text{s}$	30	V
E_{AS}	Single Pulse Avalanche Energy②	114	
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

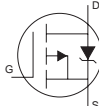
	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient⑤	—	62.5	°C/W



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.054	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.095	0.105	Ω	$V_{GS} = -10V, I_D = -3.4A$ ④
		—	0.150	0.170		$V_{GS} = -4.5V, I_D = -2.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	3.3	—	—	S	$V_{DS} = -10V, I_D = -3.1A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-2.0	μA	$V_{DS} = -55V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -55V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	26	38	nC	$I_D = -3.1A$
Q_{gs}	Gate-to-Source Charge	—	3.0	4.5		$V_{DS} = -44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	8.4	13		$V_{GS} = -10V$, See Fig. 10 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	22	ns	$V_{DD} = -28V$
t_r	Rise Time	—	10	15		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	43	64		$R_G = 6.0\Omega$
t_f	Fall Time	—	22	32		$R_D = 16\Omega$, ④
C_{iss}	Input Capacitance	—	690	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	210	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	86	—		$f = 1.0\text{MHz}$, See Fig. 9

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-27		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	54	80	ns	$T_J = 25^\circ\text{C}, I_F = -2.0A$
Q_{rr}	Reverse Recovery Charge	—	85	130	nC	$di/dt = -100A/\mu s$ ③

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 20\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = -3.4A$. (See Figure 8)

③ $I_{SD} \leq -3.4A$, $di/dt \leq -150A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ When mounted on 1 inch square copper board, $t < 10$ sec

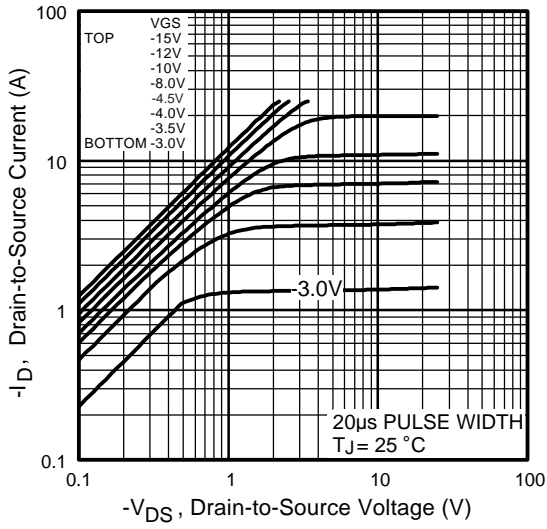


Fig 1. Typical Output Characteristics

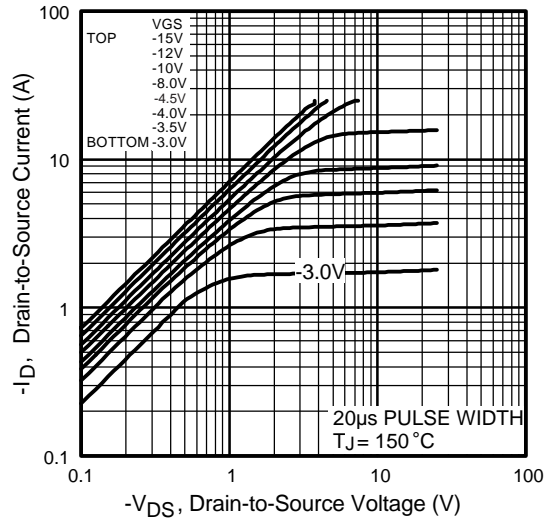


Fig 2. Typical Output Characteristics

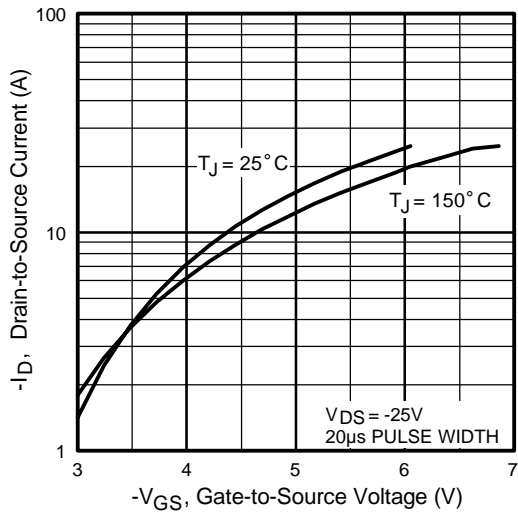


Fig 3. Typical Transfer Characteristics

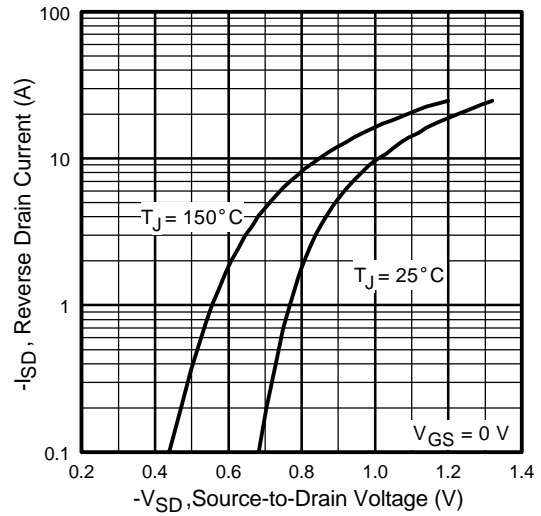


Fig 4. Typical Source-Drain Diode Forward Voltage

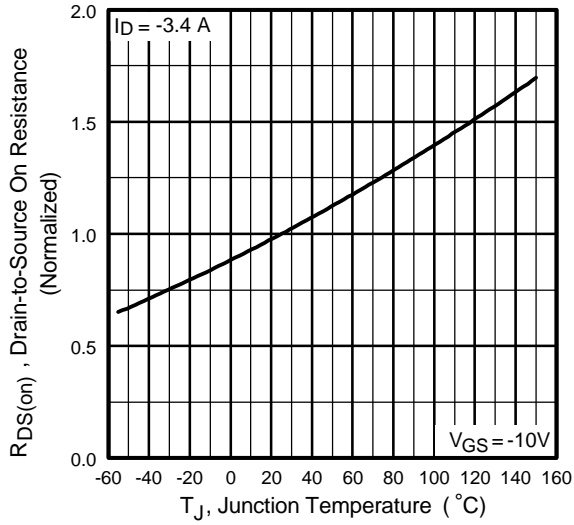


Fig 5. Normalized On-Resistance Vs. Temperature

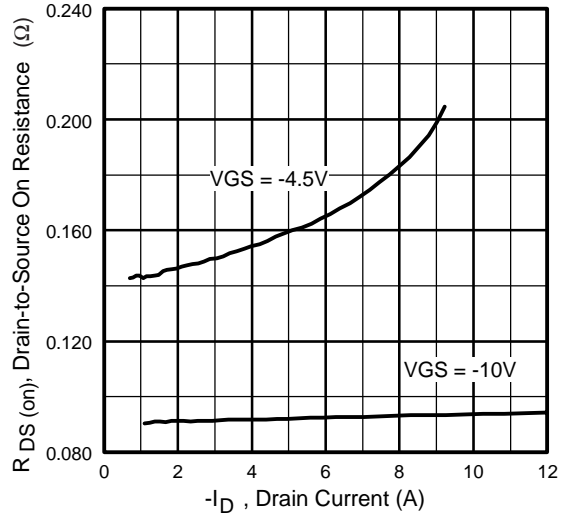


Fig 6. Typical On-Resistance Vs. Drain Current

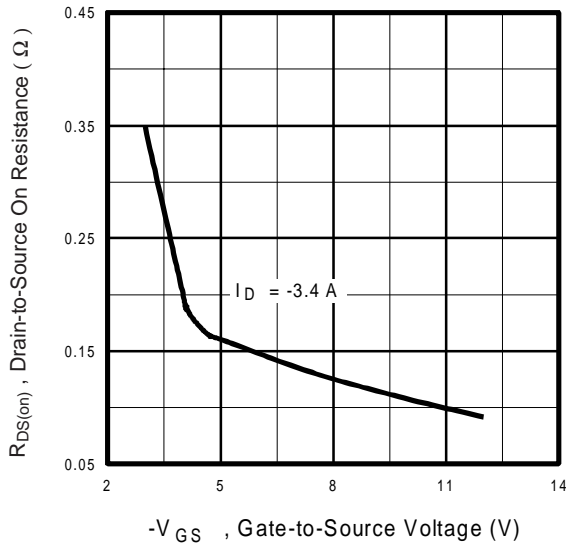


Fig 7. Typical On-Resistance Vs. Gate Voltage

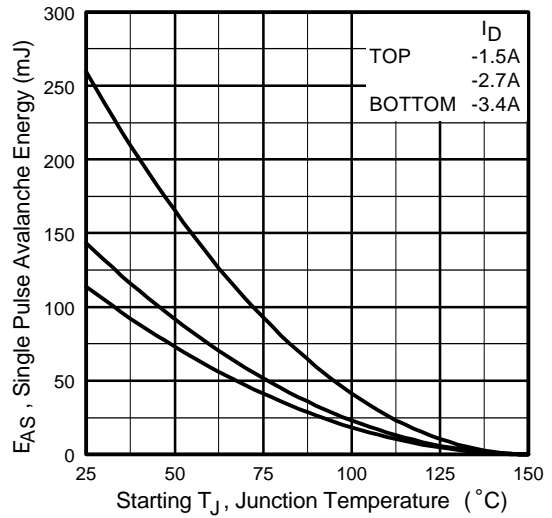


Fig 8. Maximum Avalanche Energy Vs. Drain Current

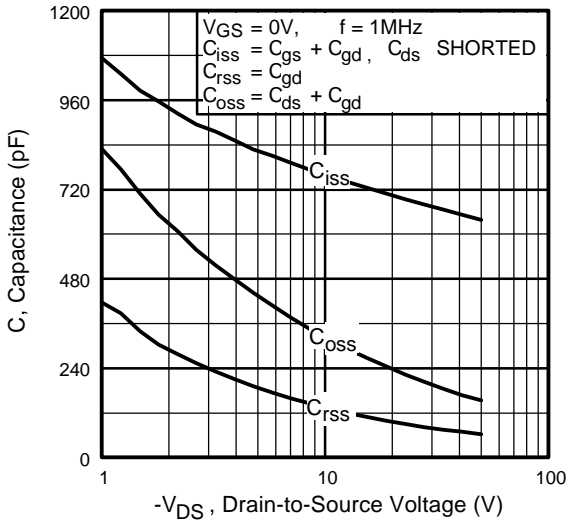


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

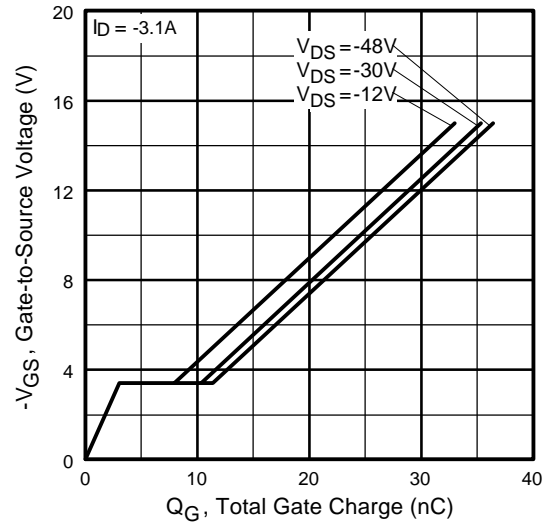


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

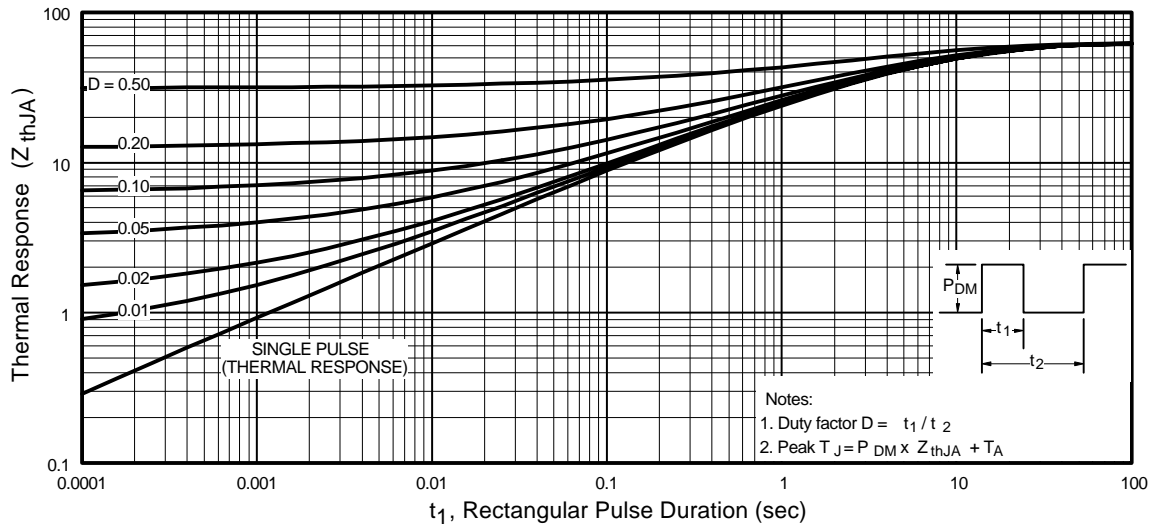
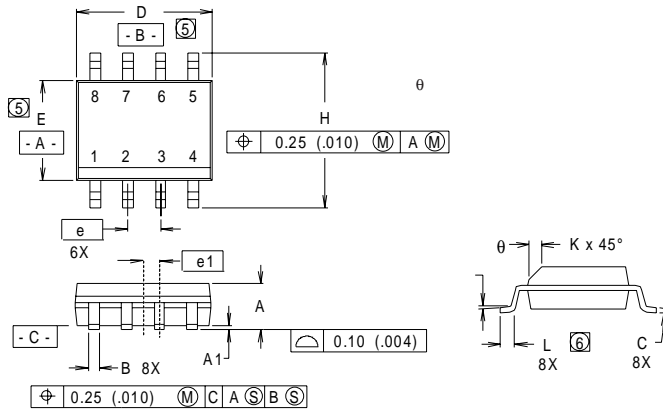


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

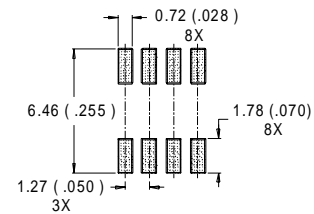
IRF7342

SO-8 Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT

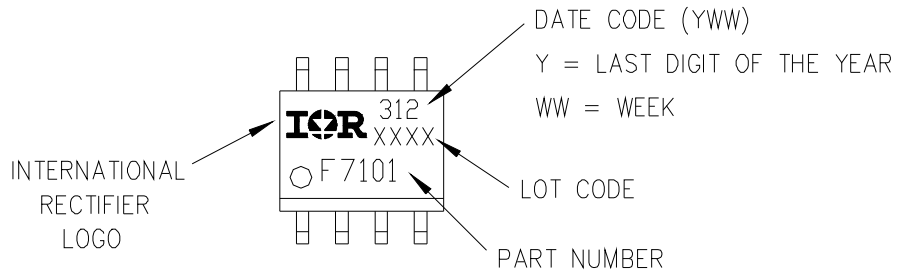


NOTES:

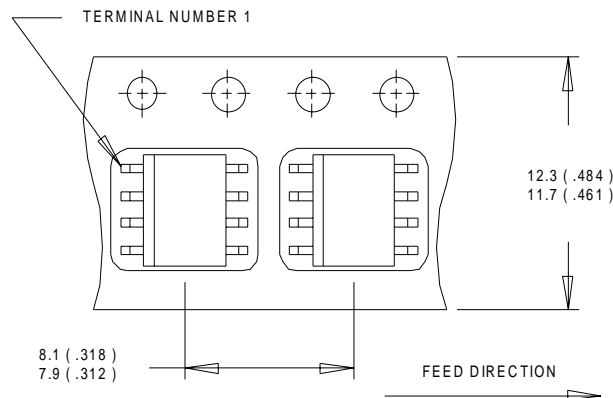
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- ⑥ DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

Part Marking

EXAMPLE: THIS IS AN IRF7101

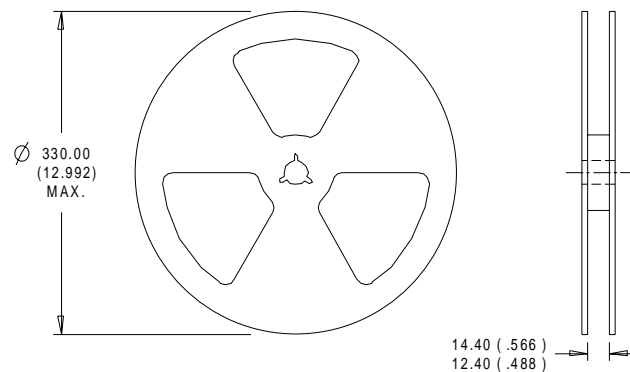


Tape and Reel



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.