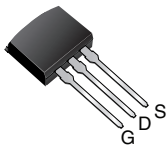


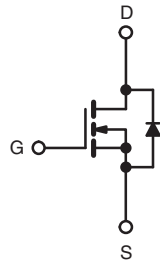
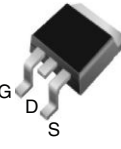
Power MOSFET

| PRODUCT SUMMARY | |
|---------------------------|-----------------------------|
| V_{DS} (V) | 500 |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ 0.85 |
| Q_g (Max.) (nC) | 38 |
| Q_{gs} (nC) | 9.0 |
| Q_{gd} (nC) | 18 |
| Configuration | Single |

I²PAK (TO-262)



D²PAK (TO-263)



N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half Bridge
- Full Bridge

| ORDERING INFORMATION | | | | |
|---------------------------------|-----------------------------|-------------------------------|-------------------------------|-----------------------------|
| Package | D ² PAK (TO-263) | D ² PAK (TO-263) | D ² PAK (TO-263) | I ² PAK (TO-262) |
| Lead (Pb)-free and Halogen-free | SiHF840AS-GE3 | SiHF840ASTRL-GE3 ^a | SiHF840ASTRR-GE3 ^a | SiHF840AL-GE3 ^a |
| Lead (Pb)-free | IRF840ASPbF | IRF840ASTRLPbF ^a | IRF840ASTRRPbF ^a | IRF840ALPbF |
| | SiHF840AS-E3 | SiHF840ASTL-E3 ^a | SiHF840ASTR-E3 ^a | SiHF840AL-E3 |

Note

a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | |
|---|------------------|-----------------------------------|---------------------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | V_{DS} | 500 | V |
| Gate-Source Voltage | V_{GS} | ± 30 | |
| Continuous Drain Current | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | 8.0 |
| | | $T_C = 100\text{ }^\circ\text{C}$ | 5.1 |
| Pulsed Drain Current ^a | I_{DM} | 32 | A |
| Linear Derating Factor | | 1.0 | W/ $^\circ\text{C}$ |
| Single Pulse Avalanche Energy ^b | E_{AS} | 510 | mJ |
| Repetitive Avalanche Current ^a | I_{AR} | 8.0 | A |
| Repetitive Avalanche Energy ^a | E_{AR} | 13 | mJ |
| Maximum Power Dissipation | P_D | $T_C = 25\text{ }^\circ\text{C}$ | 125 |
| | | $T_A = 25\text{ }^\circ\text{C}$ | 3.1 |
| Peak Diode Recovery dV/dt ^c | dV/dt | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 150 | $^\circ\text{C}$ |
| Soldering Temperature | for 10 s | 300 ^d | |

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 16\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 8.0\text{ A}$ (see fig. 12).
- $I_{SD} \leq 8.0\text{ A}$, $dI/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Uses IRF840A, SiHF840A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | | |
|--|-------------------|------|------|------|------|
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R _{thJA} | - | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R _{thJC} | - | - | 1.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

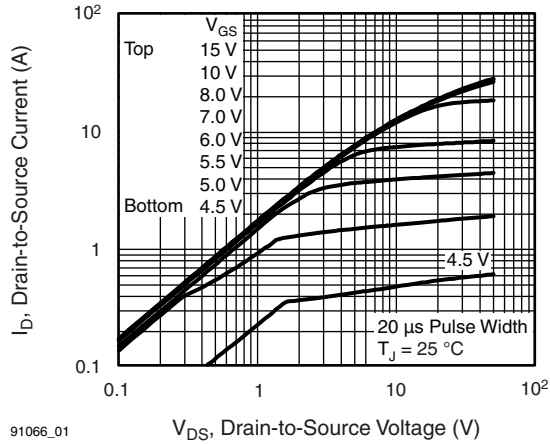
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | |
|---|----------------------------------|--|---|------|------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0, I _D = 250 μA | | 500 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA ^d | | - | 0.58 | - | V/°C |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 30 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 500 V, V _{GS} = 0 V | | - | - | 25 | μA |
| | | V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 4.8 A ^b | - | - | 0.85 | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 50 V, I _D = 4.8 A | | 3.7 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 | | - | 1018 | - | pF |
| Output Capacitance | C _{oss} | | | - | 155 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 8.0 | - | |
| Output Capacitance | C _{oss} | V _{GS} = 0 V | V _{DS} = 1.0 V, f = 1.0 MHz | 1490 | - | - | |
| Output Capacitance | C _{oss} | | V _{DS} = 400 V, f = 1.0 MHz | 42 | - | - | |
| Effective Output Capacitance | C _{oss eff.} | | V _{DS} = 0 V to 480 V ^{c, d} | 56 | - | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 8.0 A, V _{DS} = 400 V, see fig. 6 and 13 ^{b, d} | - | - | 38 | nC |
| Gate-Source Charge | Q _{gs} | | | - | - | 9.0 | |
| Gate-Drain Charge | Q _{gd} | | | - | - | 18 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 250 V, I _D = 8.0 A, R _g = 9.1 Ω, R _D = 31 Ω, see fig. 10 ^{b, d} | | - | 11 | - | ns |
| Rise Time | t _r | | | - | 23 | - | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 26 | - | |
| Fall Time | t _f | | | - | 19 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 8.0 | A |
| Pulsed Diode Forward Current ^a | I _{SM} | | | - | - | 32 | |
| Body Diode Voltage | V _{SD} | T _J = 25 °C, I _S = 8.0 A, V _{GS} = 0 V ^b | | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = 8.0 A, di/dt = 100 A/μs ^b | | - | 422 | 633 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | - | 2.0 | 3.0 | μC |
| Forward Turn-On Time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D) | | | | | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
- Uses IRF840A, SiHF840A data and test conditions

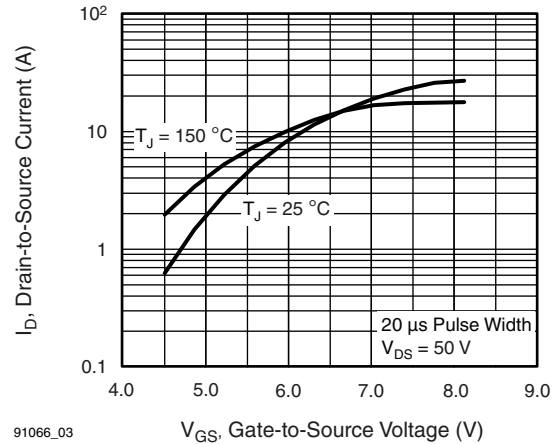


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



91066_01

Fig. 1 - Typical Output Characteristics



91066_03

Fig. 3 - Typical Transfer Characteristics



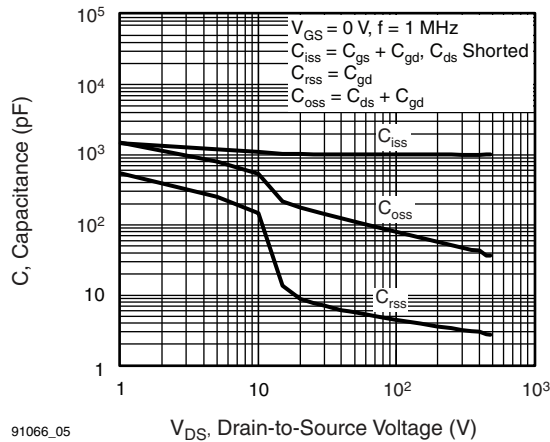
91066_02

Fig. 2 - Typical Output Characteristics



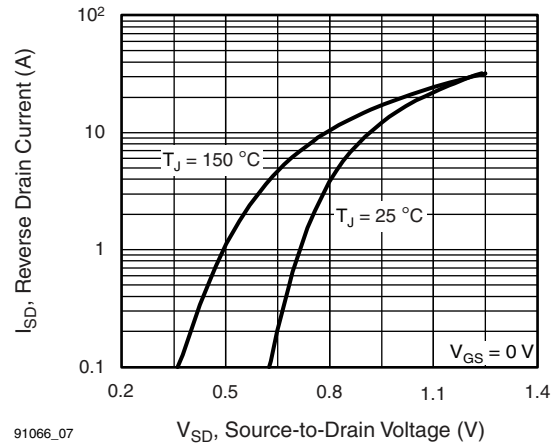
91066_04

Fig. 4 - Normalized On-Resistance vs. Temperature



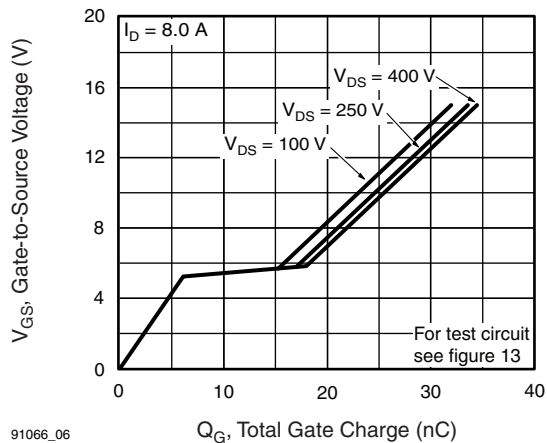
91066_05

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



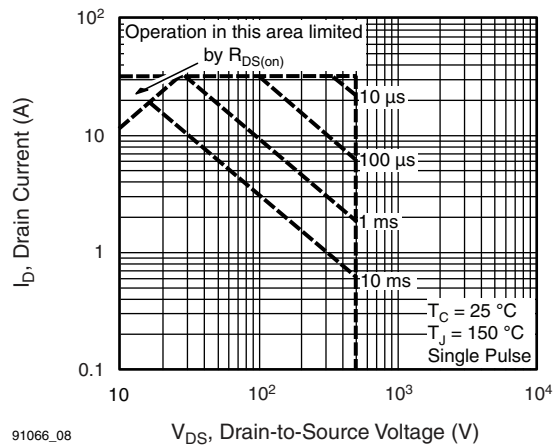
91066_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



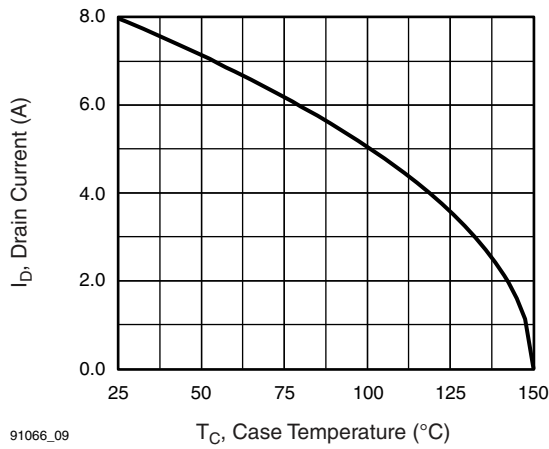
91066_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91066_08

Fig. 8 - Maximum Safe Operating Area



91066_09

Fig. 9 - Maximum Drain Current vs. Case Temperature

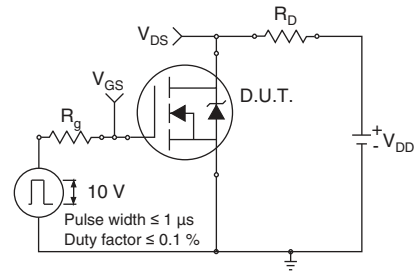


Fig. 10a - Switching Time Test Circuit

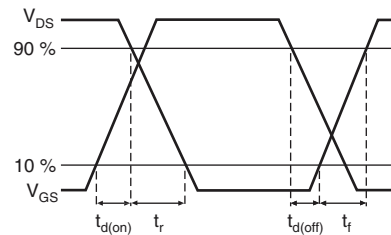
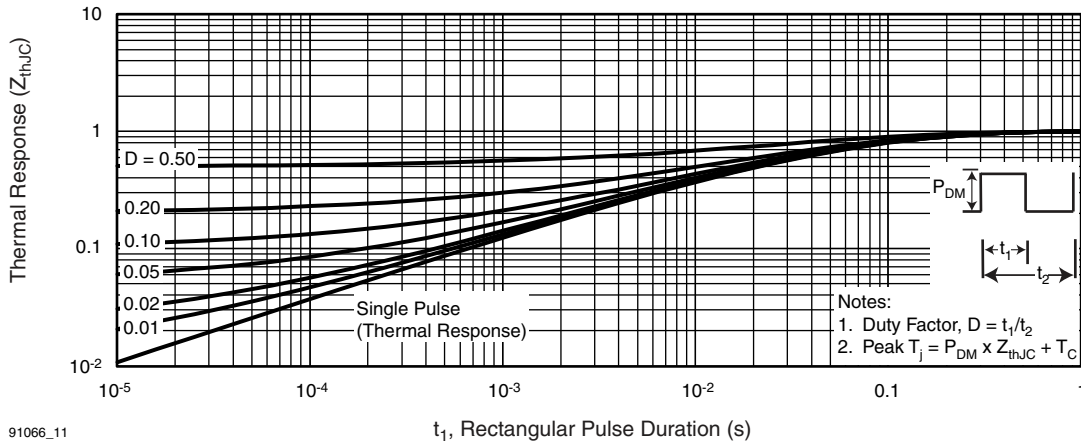


Fig. 10b - Switching Time Waveforms



91066_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

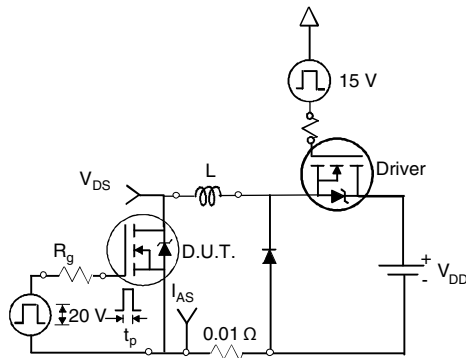


Fig. 12a - Unclamped Inductive Test Circuit

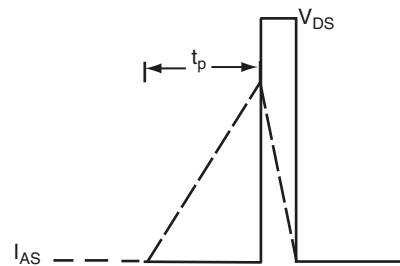


Fig. 12b - Unclamped Inductive Waveforms

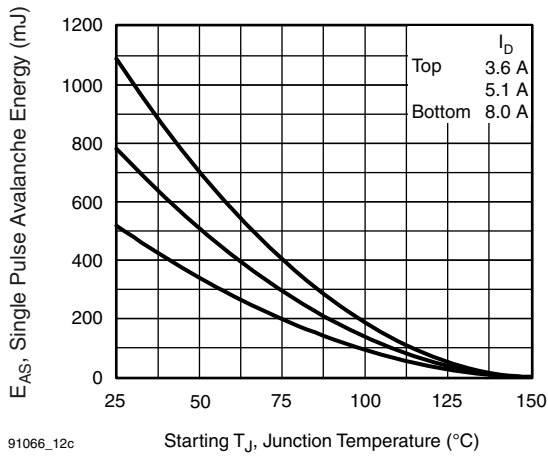


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

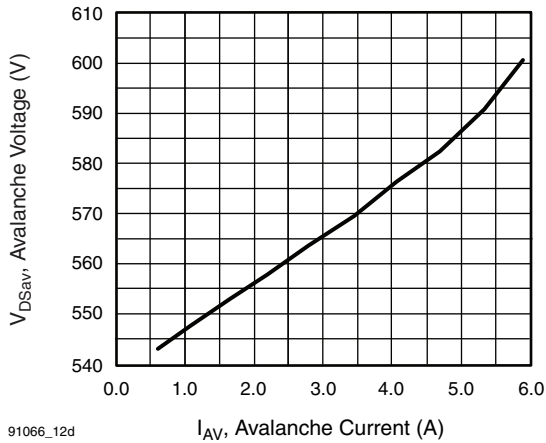


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

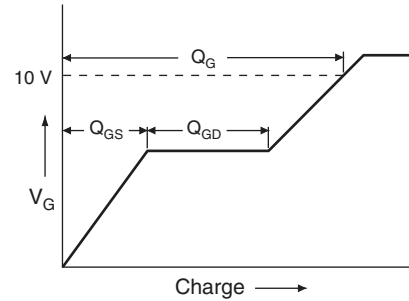


Fig. 13a - Basic Gate Charge Waveform

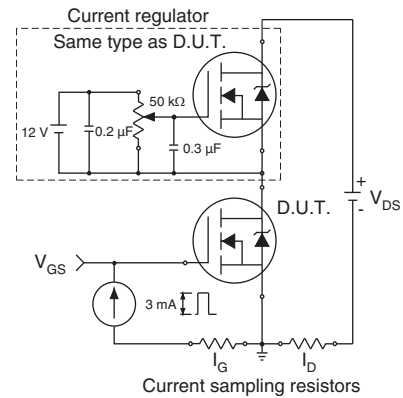


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



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