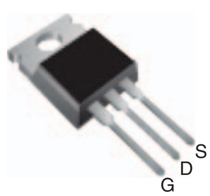
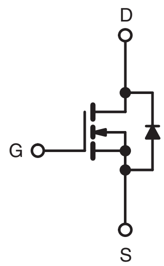
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 600 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 4.4 |
| $Q_g$ (Max.) (nC) | 18 | |
| $Q_{gs}$ (nC) | 3.0 | |
| $Q_{gd}$ (nC) | 8.9 | |
| Configuration | Single | |

TO-220




N-Channel MOSFET

## FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Available
RoHS*
COMPLIANT

## DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

| ORDERING INFORMATION | |
|---|---|
| Package | TO-220 |
| Lead (Pb)-free | IRFBC20PbF |
| | SiHFBC20-E3 |
| SnPb | IRFBC20 |
| | SiHFBC20 |

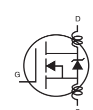
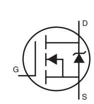
**ABSOLUTE MAXIMUM RATINGS** $T_C$ = 25 °C, unless otherwise noted

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 600 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 2.2 | A |
| | | $T_C$ = 100 °C | | 1.4 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 8.0 | |
| Linear Derating Factor | | | | 0.40 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 84 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | 2.2 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 5.0 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 50 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 3.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |
| Mounting Torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 31 mH, $R_G$ = 25 Ω, $I_{AS}$ = 2.2 A (see fig. 12).
c. $I_{SD} \leq 2.2$ A, dI/dt ≤ 40 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | |
| Case-to-Sink, Flat, Greased Surface | $R_{thCS}$ | 0.50 | - | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 2.5 | |

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 600 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.88 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | - | - | 100 | µA |
| | | $V_{DS}$ = 480V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 500 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V; $I_D$ = 1.3 A[b] | - | - | 4.4 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 1.3 A[b] | 1.4 | - | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | | - | 350 | - | |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | - | 48 | - | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 8.6 | - | |
| Total Gate Charge | $Q_g$ | | - | - | 18 | |
| Gate-Source Charge | $Q_{gs}$ | $V_{GS}$ = 10 V; $I_D$ = 2.0 A, $V_{DS}$ = 360 V see fig. 6 and 13[b] | - | - | 3.0 | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | - | 8.9 | |
| Turn-On Delay Time | $t_{d(on)}$ | | - | 10 | - | |
| Rise Time | $t_r$ | $V_{DD}$ = 300 V, $I_D$ = 2.0 A, $R_G$ = 18 Ω, $R_D$= 150 Ω see fig. 10[b] | - | 23 | - | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 30 | - | |
| Fall Time | $t_f$ | | - | 25 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 2.2 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | - | - | 8.0 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 2.2 A, $V_{GS}$ = 0 V[b] | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 2.0 A, dI/dt = 100 A/µs[b] | - | 290 | 580 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 0.67 | 1.3 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

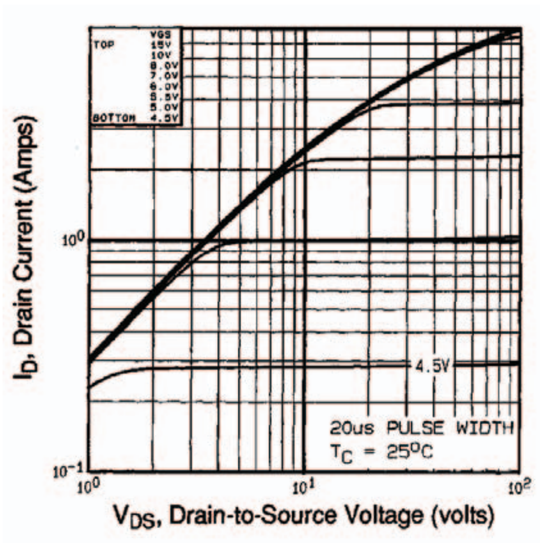



Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C

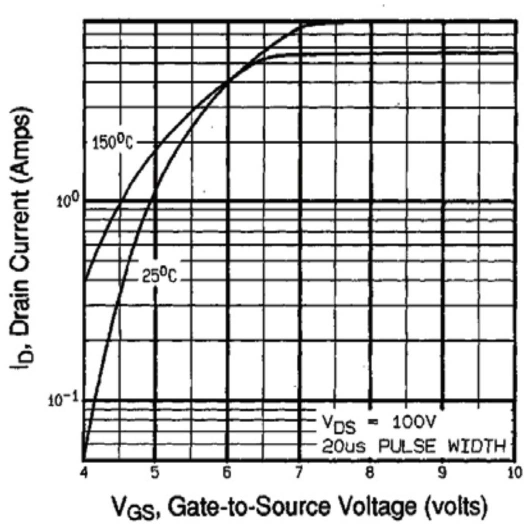



Fig. 3 - Typical Transfer Characteristics

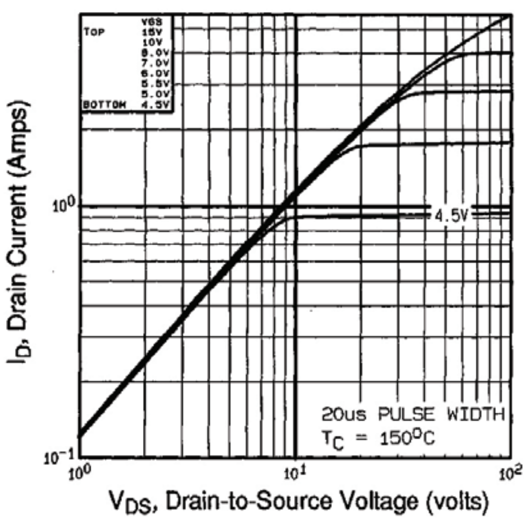



Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C

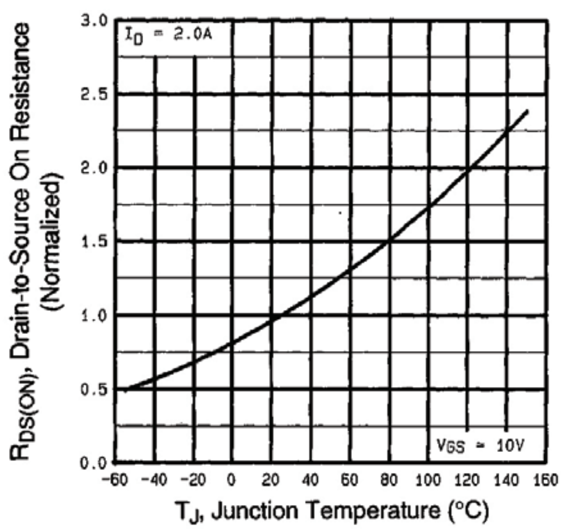



Fig. 4 - Normalized On-Resistance vs. Temperature

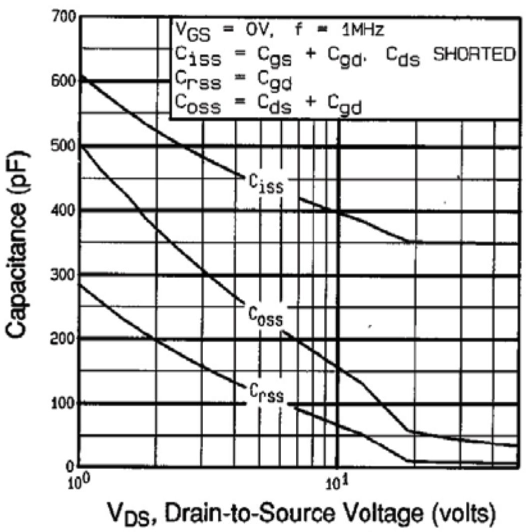



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

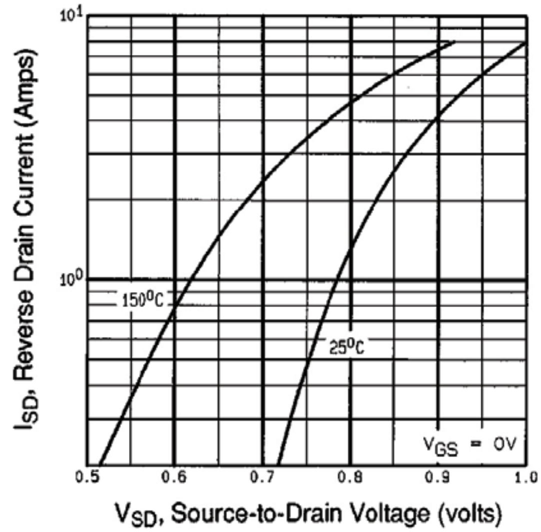



Fig. 7 - Typical Source-Drain Diode Forward Voltage

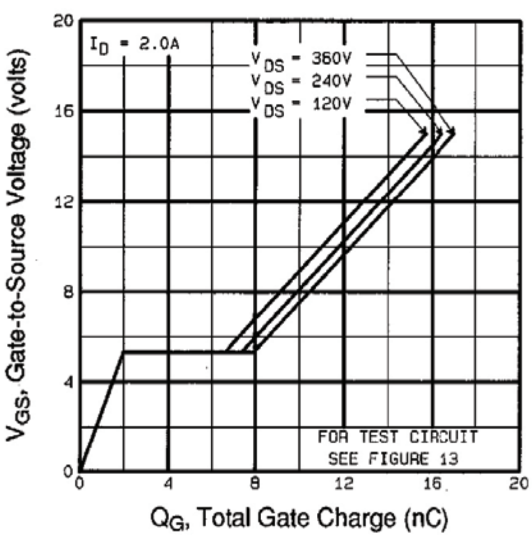



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

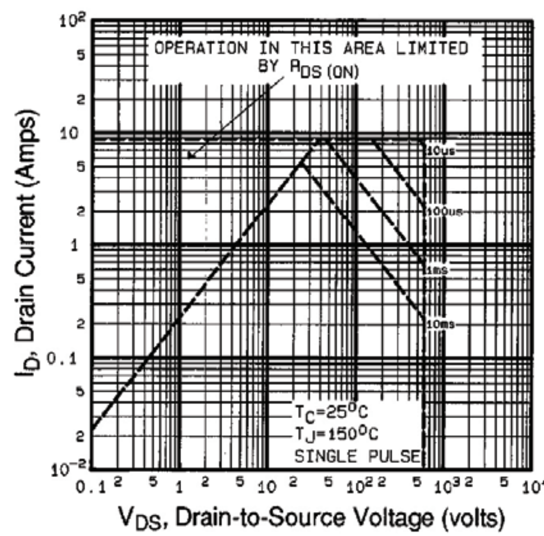



Fig. 8 - Maximum Safe Operating Area

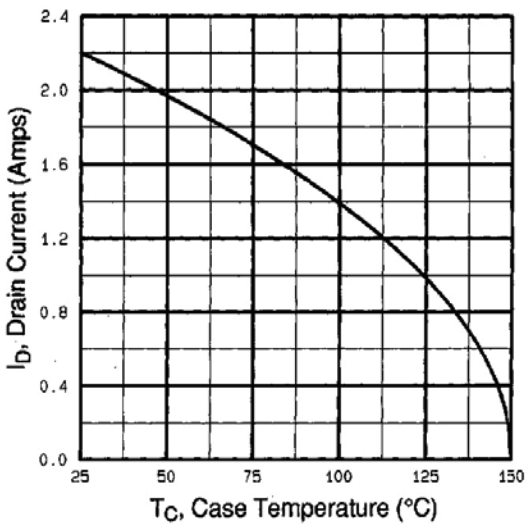



Fig. 9 - Maximum Drain Current vs. Case Temperature

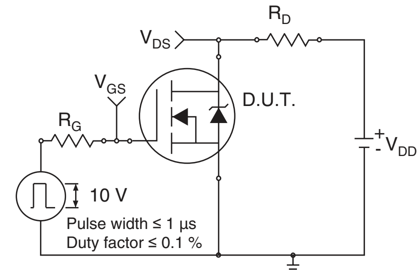



Fig. 10a - Switching Time Test Circuit

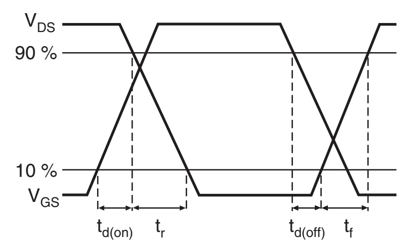



Fig. 10b - Switching Time Waveforms

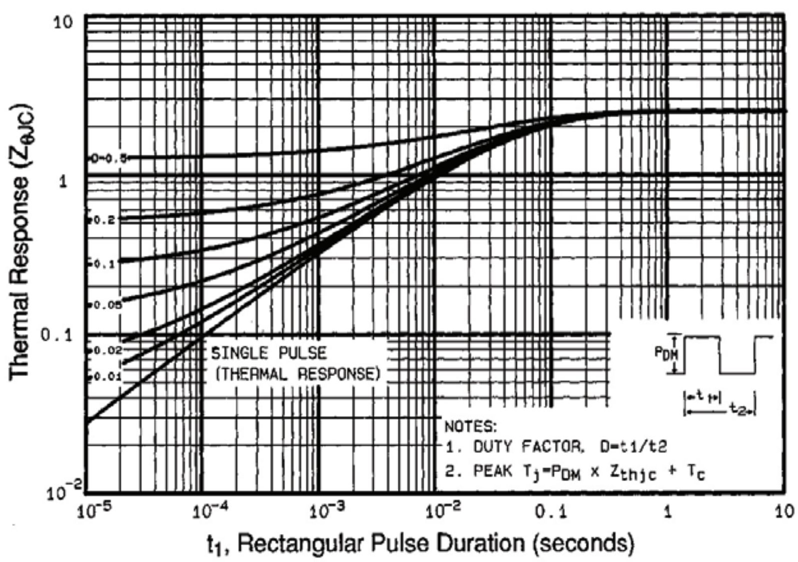



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

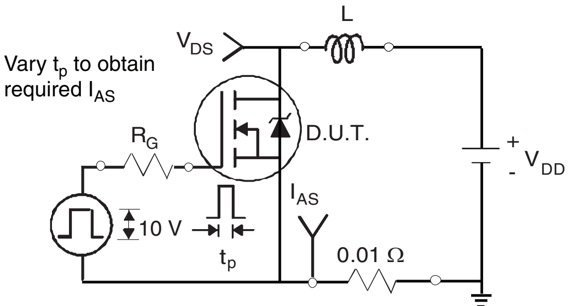



**Fig. 12a - Unclamped Inductive Test Circuit**

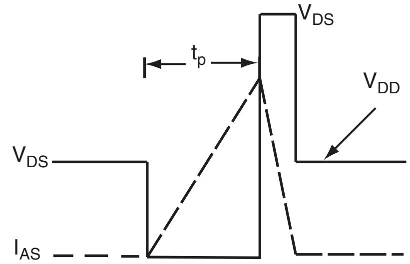



**Fig. 12b - Unclamped Inductive Waveforms**

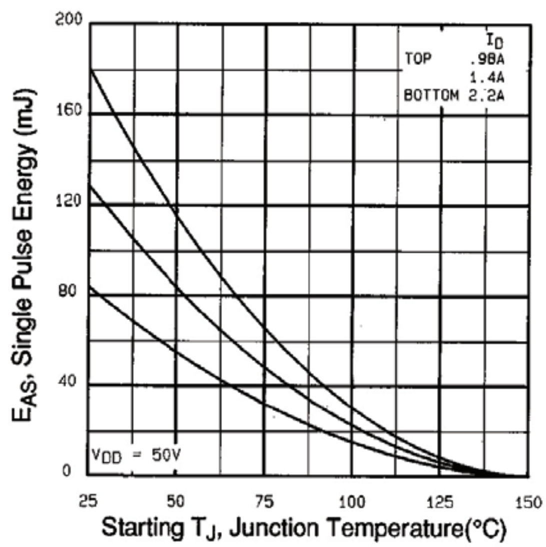



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

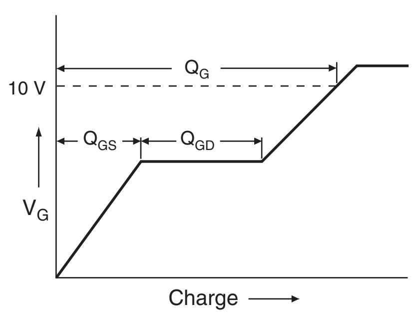



**Fig. 13a - Basic Gate Charge Waveform**

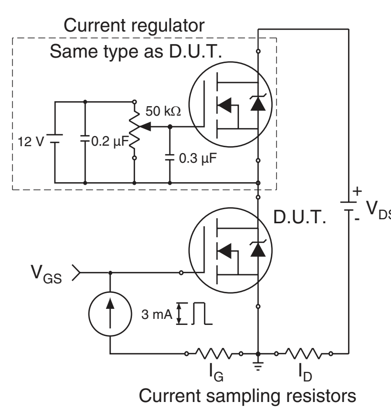
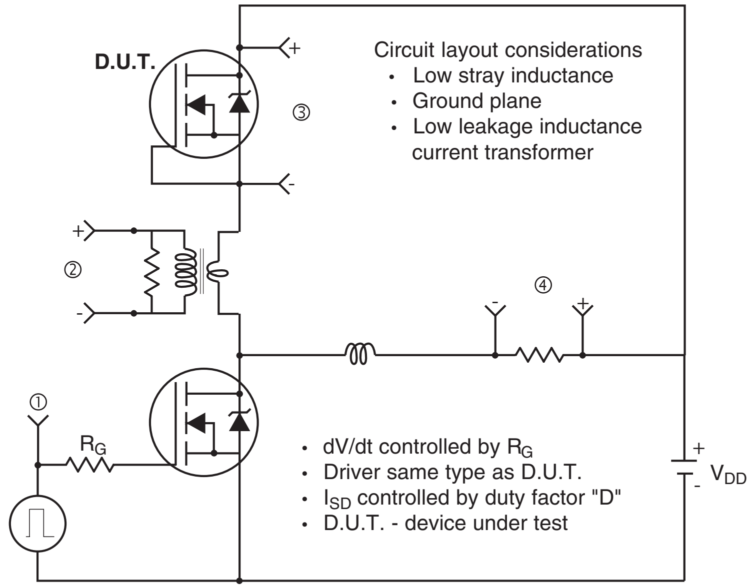
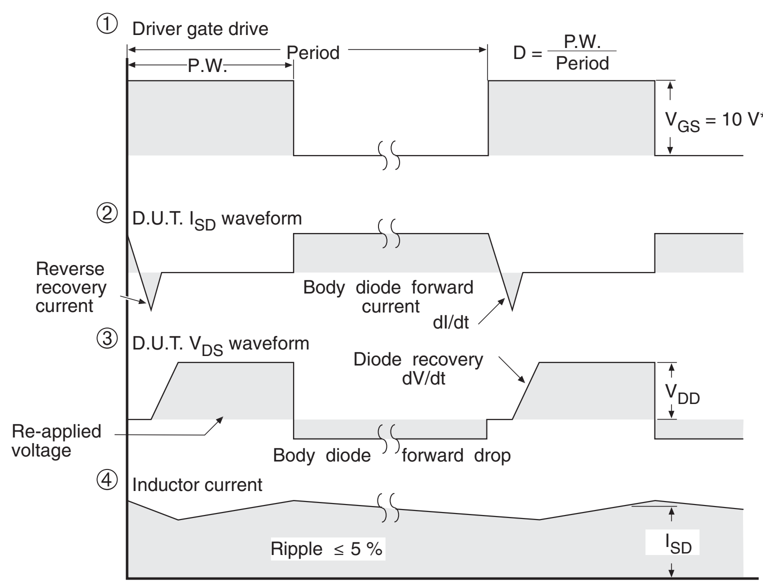



**Fig. 13b - Gate Charge Test Circuit**

## Peak Diode Recovery dV/dt Test Circuit




* $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

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