MAC15SD, MAC15SM, MAC15SN

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

- Sensitive Gate allows Triggering by Microcontrollers and other Logic Circuits
- High Immunity to dv/dt - 25 V/µs minimum at 110°C
- High Commutating di/dt - 8.0 A/ms minimum at 110°C
- Maximum Values of I_{GT}, V_{GT} and I_H Specified for Ease of Design
- On-State Current Rating of 15 A RMS at 70°C
- High Surge Current Capability - 120 A
- Blocking Voltage to 800 V
- Rugged, Economical TO220AB Package
- Uniform Gate Trigger Currents in Three Quadrants, Q1, Q2, and Q3
- Device Marking: Logo, Device Type, e.g., MAC15SD, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T_J = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) MAC15SD MAC15SM MAC15SN	V_{DRM}, V_{RRM}	400 600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60Hz, T_J = 70°C)	$I_{T(RMS)}$	15	A
Peak Non-repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J = 110°C)	I_{TSM}	120	A
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	60	A^2s
Peak Gate Power (Pulse Width ≤ 1.0 µs, T_C = 70°C)	P_{GM}	20	W
Average Gate Power (t = 8.3 ms, T_C = 70°C)	$P_{G(AV)}$	0.5	W
Operating Junction Temperature Range	T_J	- 40 to +110	°C
Storage Temperature Range	T_{stg}	- 40 to +150	°C

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.
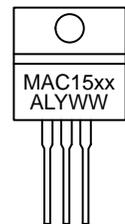
ON Semiconductor

http://onsemi.com

TRIACS
15 AMPERES RMS
400 thru 800 VOLTS

MT2 o———————o MT1
G

MARKING DIAGRAM

MAC15xx
ALYWW
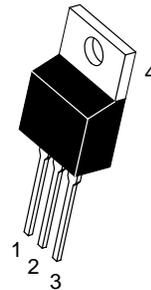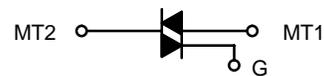
TO-220AB
CASE 221A
Style 4

xx = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week

PIN ASSIGNMENT

1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC15SD	TO220AB	50 Units/Rail
MAC15SM	TO220AB	50 Units/Rail
MAC15SN	TO220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

MAC15SD, MAC15SM, MAC15SN

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance - Junction to Case - Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

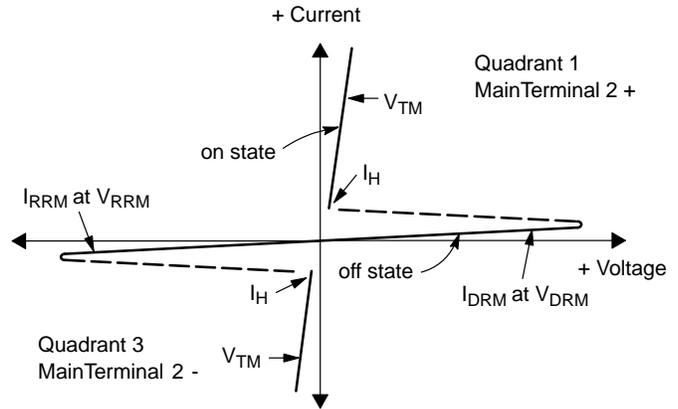| Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					

Peak Repetitive Blocking Current
  (V_D = Rated V_{DRM}, V_{RRM}; Gate Open) T_J = 25°C
                                                                                      T_J = 110°C
	I_{DRM},
	I_{RRM}
		-
		-
			-
			-
				0.01
				2.0
					mA

ON CHARACTERISTICS					
Peak On-State Voltage[1] ($I_{TM} = \pm 21A$)	V_{TM}	-	-	1.8	V

Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100Ω)
  MT2(+), G(+)
  MT2(+), G(-)
  MT2(-), G(-)
	I_{GT}	-
		-
		-
			2.0
			3.0
			3.0
				5.0
				5.0
				5.0
					mA

Hold Current (V_D = 12 V, Gate Open, Initiating Current = $\pm 150mA$)	I_H	-	3.0	10	mA

Latching Current (V_D = 24V, I_G = 5mA)
  MT2(+), G(+)
  MT2(+), G(-)
  MT2(-), G(-)
	I_L	-
		-
		-
			5.0
			10
			5.0
				15
				20
				15
					mA

Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100Ω)
  MT2(+), G(+)
  MT2(+), G(-)
  MT2(-), G(-)
	V_{GT}	0.45
		0.45
		0.45
			0.62
			0.60
			0.65
				1.5
				1.5
				1.5
					V

DYNAMIC CHARACTERISTICS					

Rate of Change of Commutating Current
  (V_D = 400V, I_{TM} = 3.5A, Commutating dv/dt = 10Vμ/sec,
  Gate Open, T_J = 110°C, f= 500Hz, Snubber: C_S = 0.01 μF, R_S =15Ω,
  see Figure 15.)
	(di/dt)c	8.0	10	-	A/ms

Critical Rate of Rise of Off-State Voltage (V_D = Rate V_{DRM}, Exponential Waveform, R_{GK} = 510Ω, T_J = 110°C)	dv/dt	25	75	-	V/μs

2. Pulse Test: Pulse Width $\leq$ 2.0 ms, Duty Cycle $\leq$ 2%.

MAC15SD, MAC15SM, MAC15SN

Voltage Current Characteristic of Triacs
(Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current

+ Current

Quadrant 1
MainTerminal 2 +

V_{TM}

on state

I_H

I_{RRM} at V_{RRM}

off state

+ Voltage

I_H

I_{DRM} at V_{DRM}

Quadrant 3
MainTerminal 2 -

V_{TM}

Quadrant Definitions for a Triac

MT2 POSITIVE
(Positive Half Cycle)
+

(+) MT2

Quadrant II

(-) I_{GT}
GATE

MT1

REF

(+) MT2

(+) I_{GT}
GATE

Quadrant I

MT1

REF

I_{GT} -

+ I_{GT}

(-) MT2

Quadrant III

(-) I_{GT}
GATE

MT1

REF

(-) MT2

(+) I_{GT}
GATE

Quadrant IV

MT1

REF

-
MT2 NEGATIVE
(Negative Half Cycle)
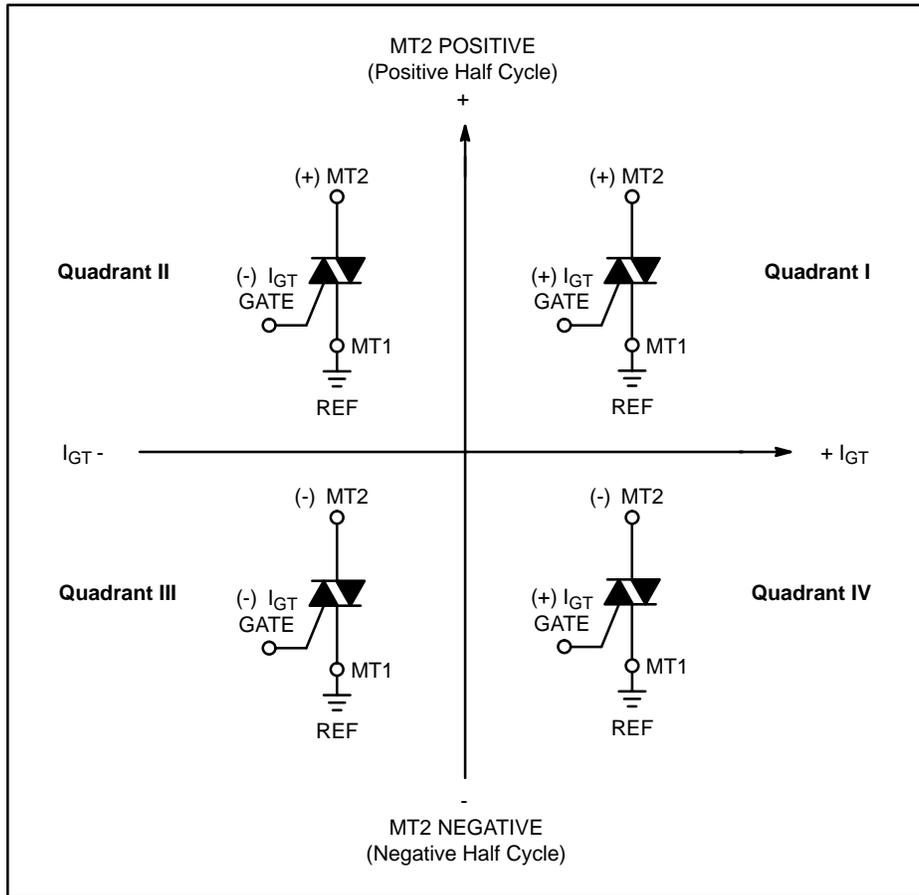
All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used.

MAC15SD, MAC15SM, MAC15SN
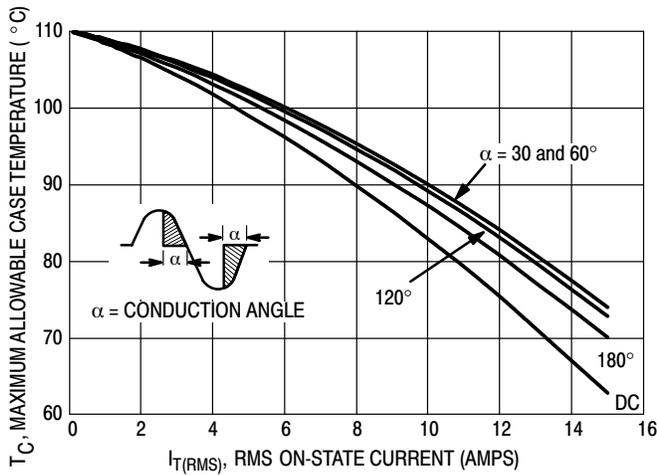
Figure 1. RMS Current Derating
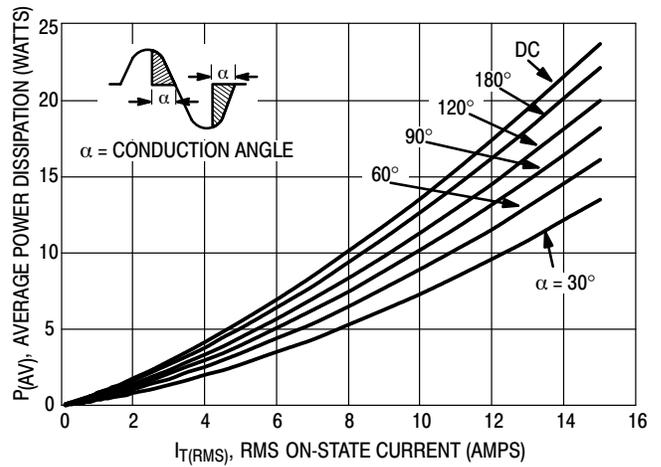
Figure 2. Maximum On-State Power Dissipation
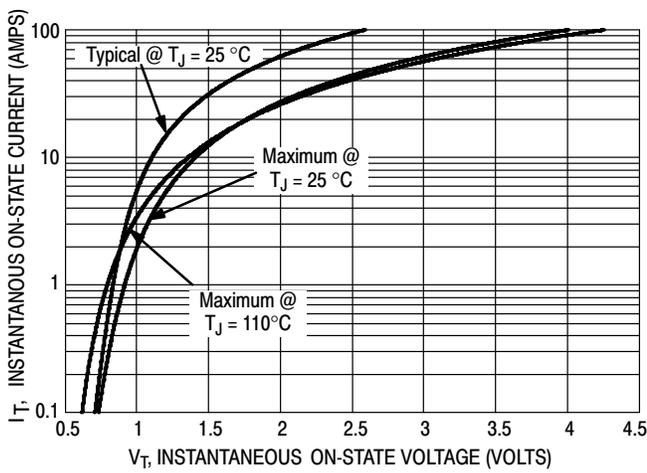
Figure 3. On-State Characteristics
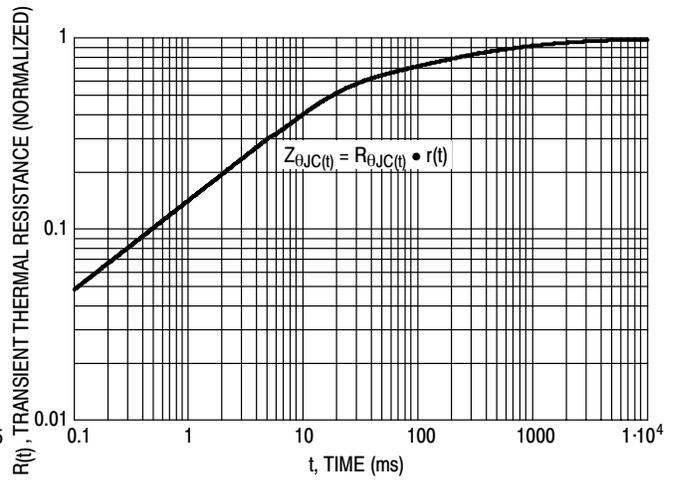
Figure 4. Transient Thermal Response

$Z_{\theta JC(t)} = R_{\theta JC(t)} \cdot r(t)$
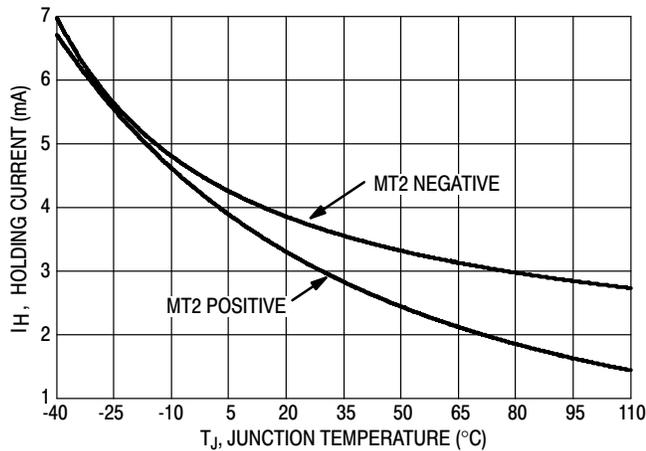
Figure 5. Typical Holding Current Versus Junction Temperature
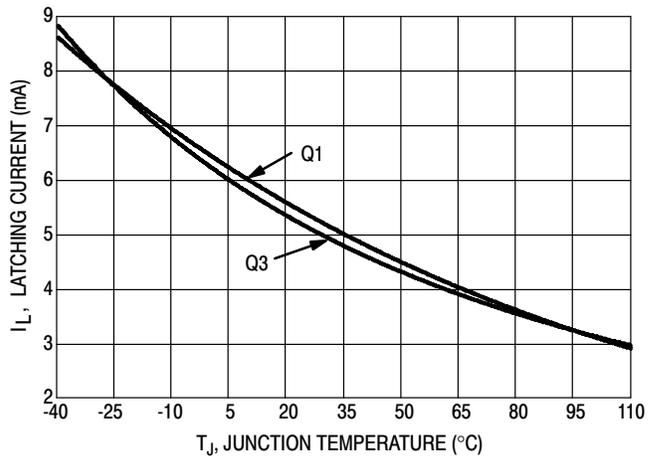
Figure 6. Typical Latching Current Versus Junction Temperature
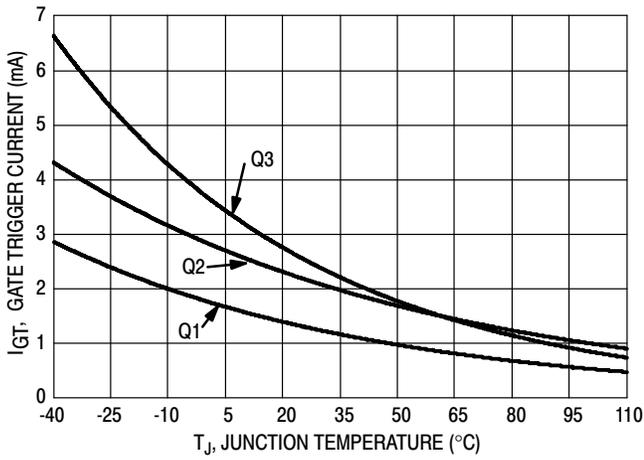
**Figure 7. Typical Gate Trigger Current
Versus Junction Temperature**
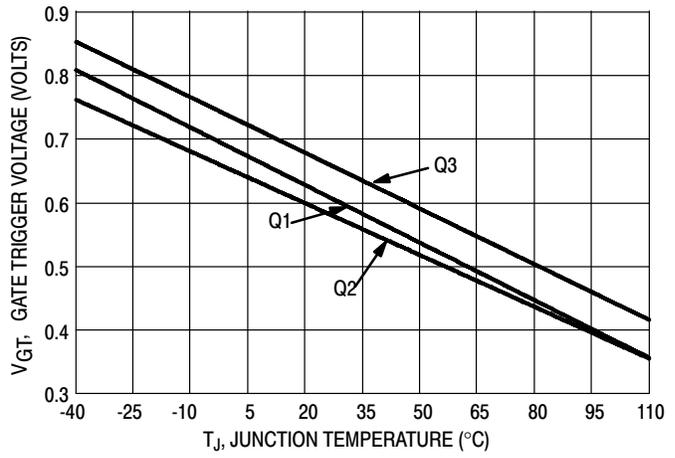
**Figure 8. Typical Gate Trigger Voltage
Versus Junction Temperature**
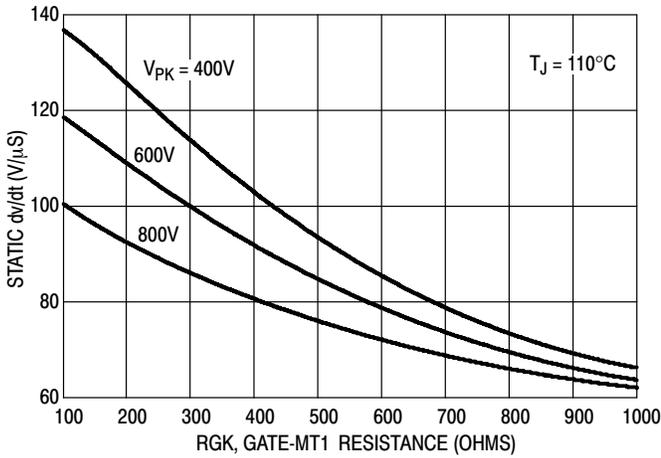
**Figure 9. Typical Exponential Static dv/dt
Versus Gate-MT1 Resistance, MT2(+)**
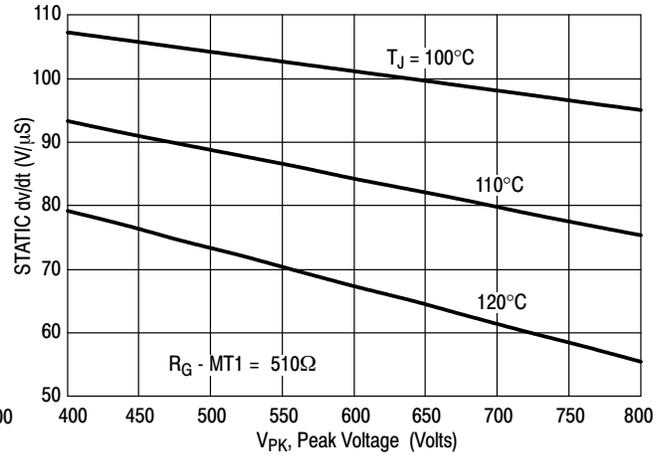
**Figure 10. Typical Exponential Static dv/dt
Versus Peak Voltage, MT2(+)**
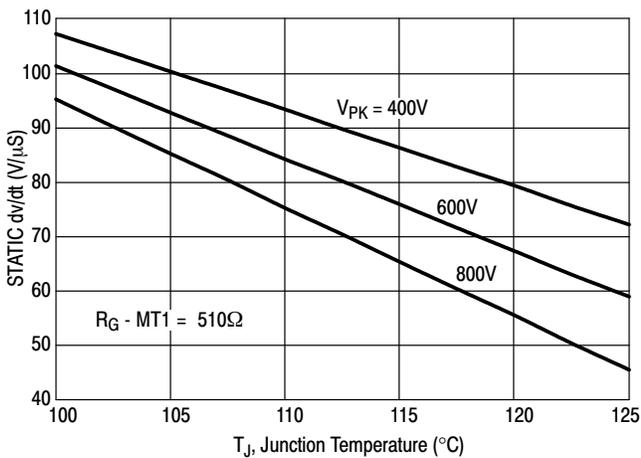
**Figure 11. Typical Exponential Static dv/dt
Versus Junction Temperature, MT2(+)**
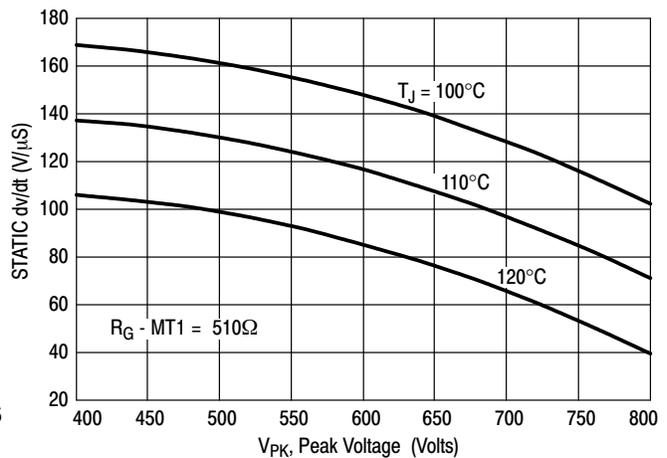
**Figure 12. Typical Exponential Static dv/dt
Versus Peak Voltage, MT2($-$)**
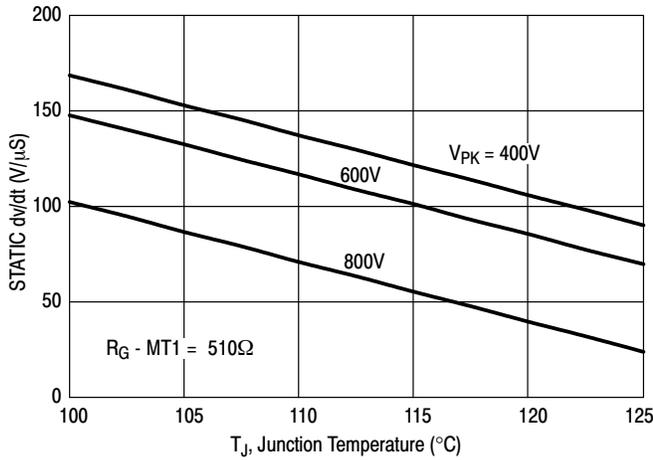
Figure 13. Typical Exponential Static dv/dt Versus Junction Temperature, MT2($-$)
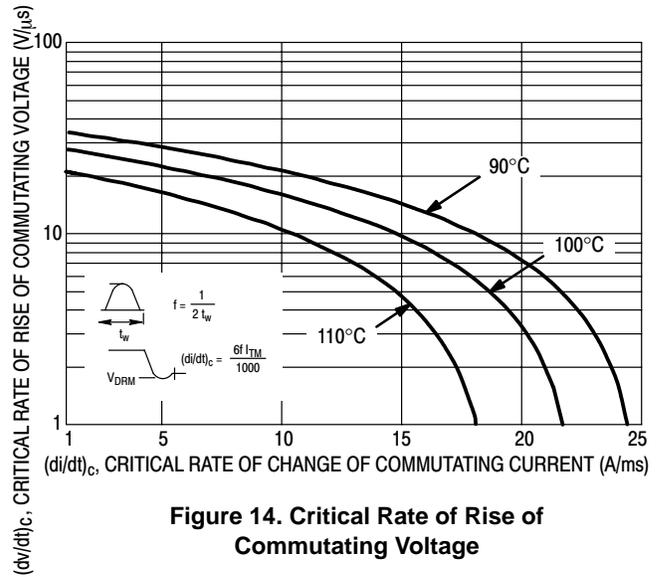
Figure 14. Critical Rate of Rise of Commutating Voltage
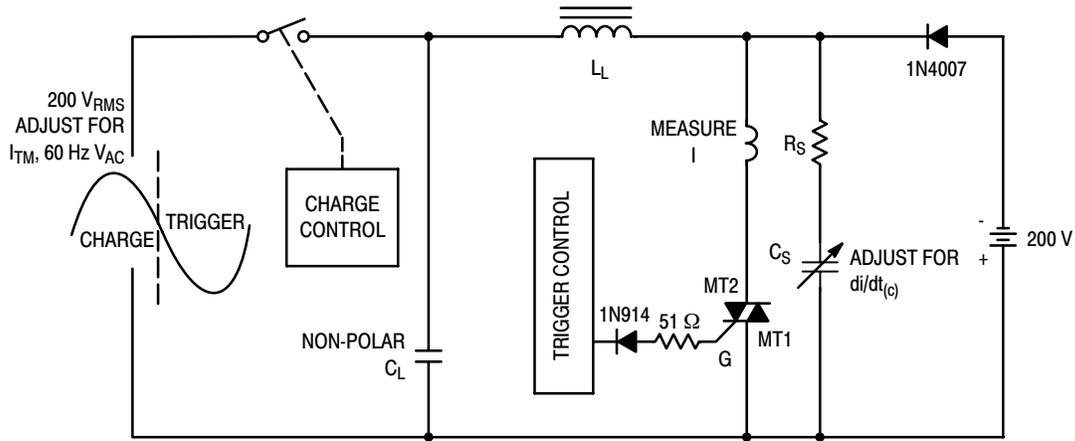
Note: Component values are for verification of rated (di/dt)$_c$. See AN1048 for additional information.

Figure 15. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current (di/dt)$_c$

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-09
ISSUE AA
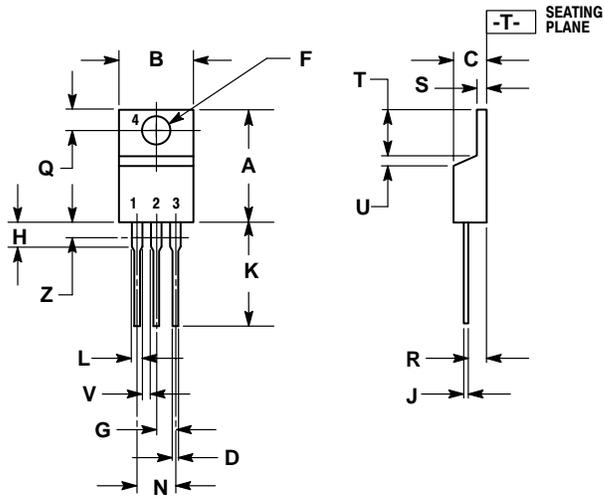
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

MAC15SD, MAC15SM, MAC15SN