2-SCART Compatible AV Switch for DVD Recorders for Europe
Monolithic IC MM1763

Outline

This IC is a one-chip IC integrating an I^2C BUS controlled AV switch with 4 inputs and 3 outputs with a 6-channel video driver with a built-in LPF. 2 outputs among 3 outputs of the AV switch are 75Ω drivers, which is ideal for analog interface for recording equipment such as 2-SCART compatible DVD recorders for Europe.

Features

1. Serially controlled with I^2C BUS
2. Provided in a small package (SSOP-42) with an extensive function of a switch + driver
3. Optimized pin assignment considering the device architecture (non-complicated board layout can be realized)
4. 6-channel video driver including a high performance 4th-order LPF
5. Audio output that is programmable between 0dB and 6dB and includes a newly-developed adjustable gain amplifier
6. Includes auto power saving function when V_{CC}=12V is off (between V_{CC}=5V, 12V)
   (when V_{CC}=12V is on, power saving is also possible by serial control)

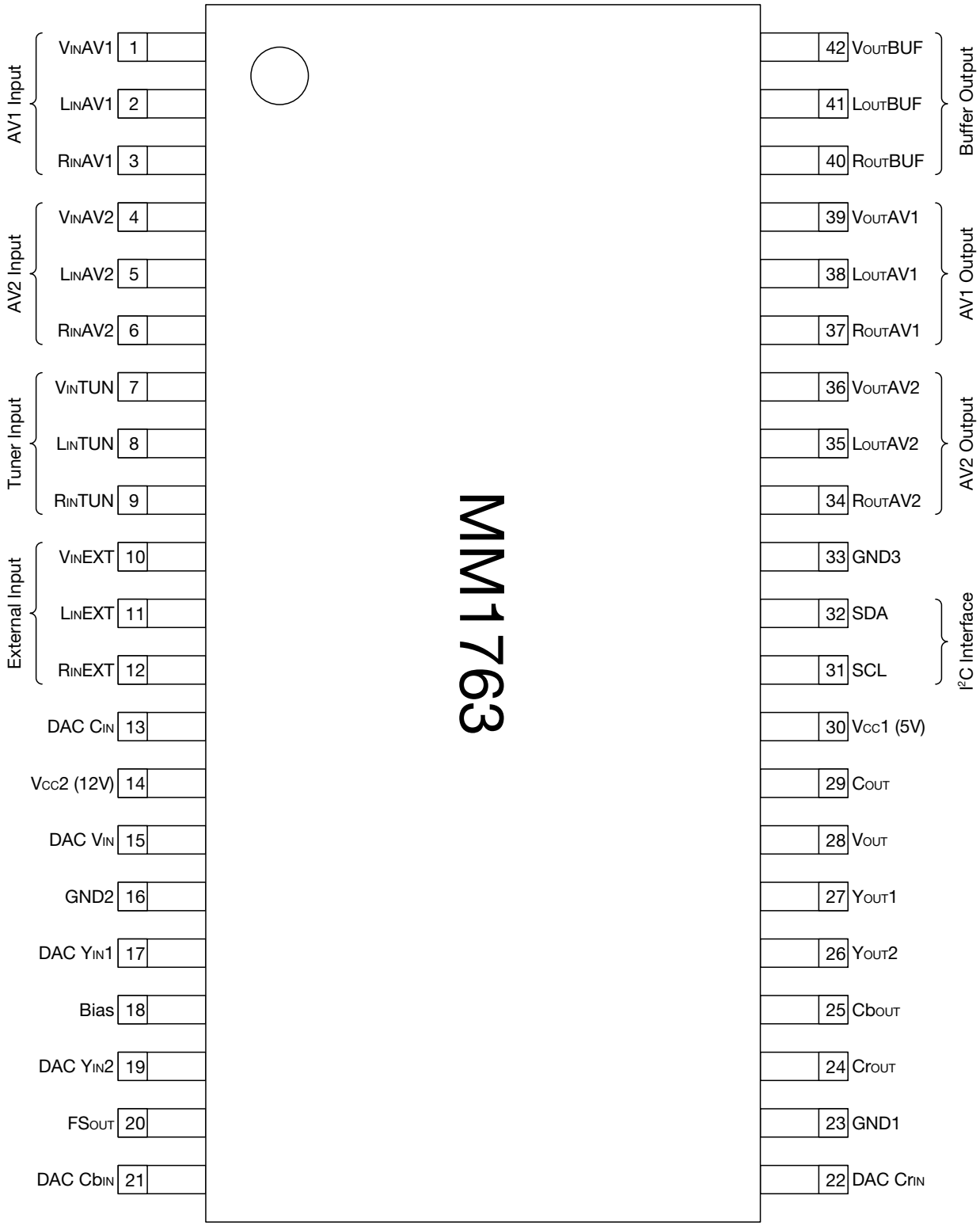
Package

SSOP-42A

Applications

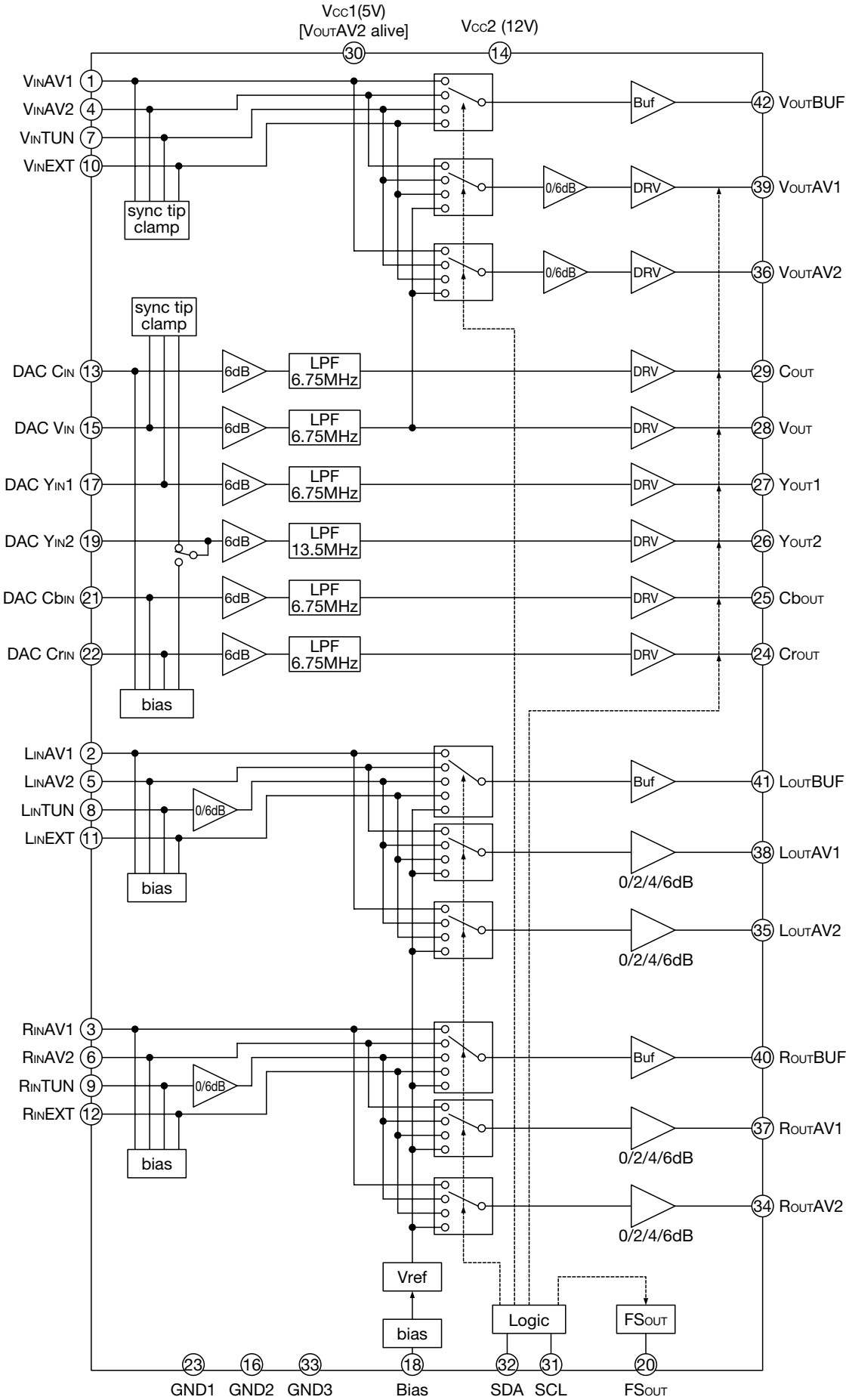
1. DVD recorders
2. VCRs
3. STBs
4. Recording equipment

Pin Assignment

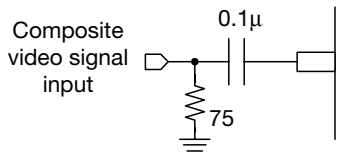


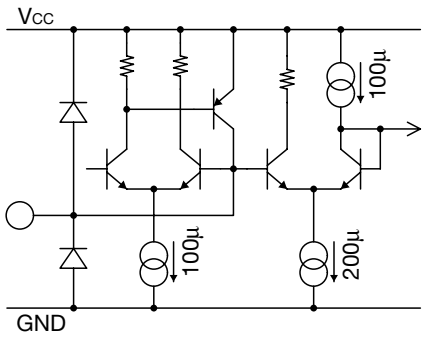
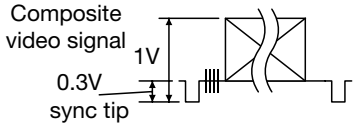
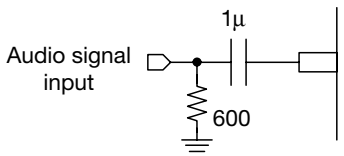
1	VINAV1	8	LINTUN	15	DAC VIN	22	DAC CrIN	29	COUT	36	VOUTAV2
2	LINAV1	9	RINTUN	16	GND2	23	GND1	30	VCC1 (5V)	37	ROUTAV1
3	RINAV1	10	VINEXT	17	DAC YIN1	24	CrOUT	31	SCL	38	LOUTAV1
4	VINAV2	11	LINEXT	18	BIAS	25	CbOUT	32	SDA	39	VOUTAV1
5	LINAV2	12	RINEXT	19	DAC YIN2	26	YOUT2	33	GND3	40	ROUTBUF
6	RINAV2	13	DAC CIN	20	FSOUT	27	YOUT1	34	ROUTAV2	41	LOUTBUF
7	VINTUN	14	VCC2 (12V)	21	DAC CbIN	28	VOUT	35	LOUTAV2	42	VOUTBUF

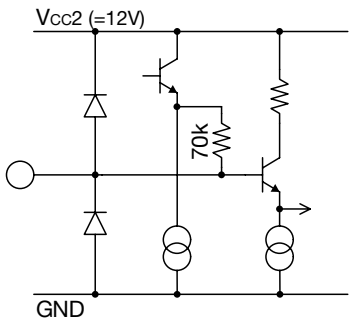
Block Diagram



Pin Description

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">1
4
7
10
15</td><td rowspan="4">VINAV1
VINAV2
VINTUN
VINEXT
DAC VIN</td><td>Function
Composite signal input
Input clamp
Pin voltage: 1.1V typ.
Input dynamic range: 1.3VP-P min.</td></tr>
<tr><td>External circuit
 

When not using it: open</td><td>Equivalent circuit diagram
 
</td></tr>
<tr><td colspan="2">Input signal
 
</td></tr>
<tr><td rowspan="4">2
3
5
6
8
9
11
12</td><td rowspan="4">LINAV1
RINAV1
LINAV2
RINAV2
LINTUN
RINTUN
LINEXT
RINEXT</td><td>Function
Audio signal input
Input impedance: 70kΩ typ.
Pin voltage: 7.0V typ.
Input dynamic range: 3Vrms min.</td></tr>
<tr><td>External circuit
 

When not using it: open</td><td>Equivalent circuit diagram
 
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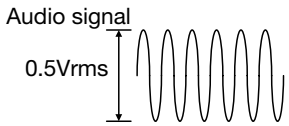
<tr><td colspan="2">Input signal
 
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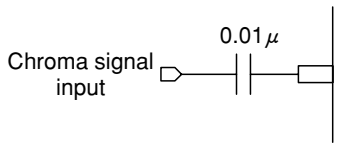
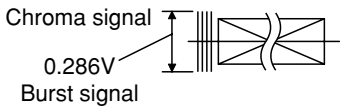
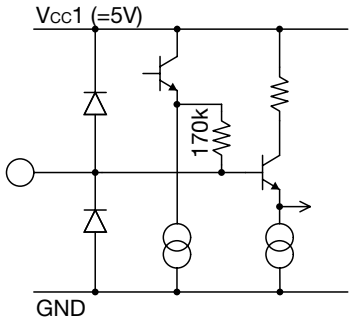
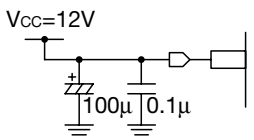
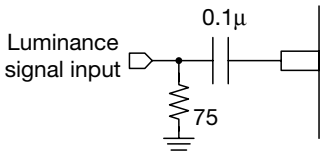
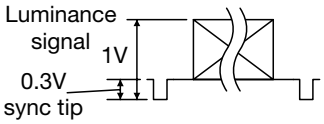
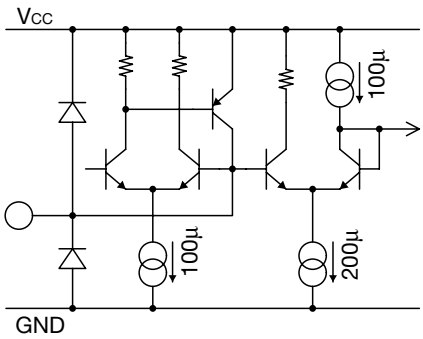
</table>

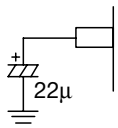
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="5">13</td><td rowspan="5">DAC C_{IN}</td><td>Function</td></tr>
<tr><td>Chroma signal input
Input bias
Pin voltage: 2.4V typ.
Input impedance: 170kΩ typ.
Input dynamic range: 1.3V_{P-P} min.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td> 

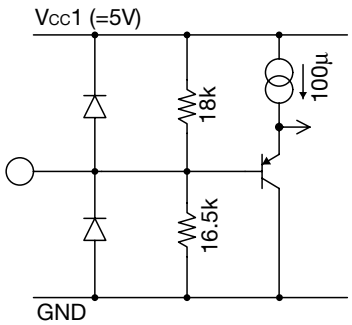
When not using it: OPEN
Output signal
 
</td><td> 
</td></tr>
<tr><td rowspan="5">14</td><td rowspan="5">Vcc2</td><td>Function</td></tr>
<tr><td>Voltage supply
It is a supply voltage impression terminal. Please impress 12V.
Please arrange a bypass capacitor near the terminal.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td> 

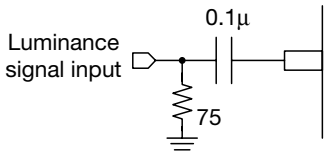
Output signal
DC voltage:
+11.2V~+12.8V</td></tr>
<tr><td rowspan="2">16
23
33</td><td rowspan="2">GND2
GND1
GND3</td><td>Function</td></tr>
<tr><td>GND
Ground</td></tr>
</table>

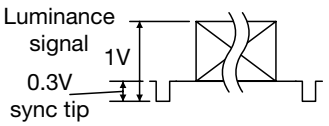
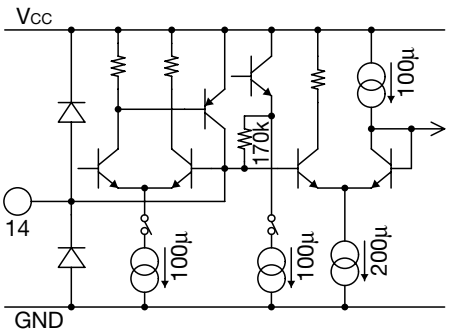
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">17</td><td rowspan="4">DAC $Y_{IN}1$</td><td>Function</td></tr>
<tr><td>Luminance signal input
Input clamp
Pin voltage: 1.1V typ.
Input dynamic range: 1.3V_{P-P} min.</td></tr>
<tr><td>External circuit
 

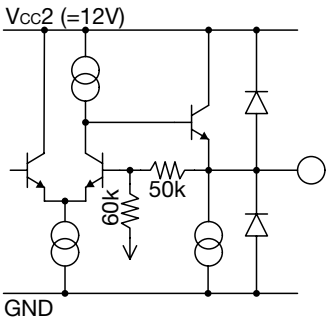
When not using it: open
Input signal
 
</td><td>Equivalent circuit diagram
 
</td></tr>
<tr><td rowspan="4">18</td><td rowspan="4">BIAS</td><td>Function</td></tr>
<tr><td>BIAS
All the reference voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor to stabilize the reference voltage.

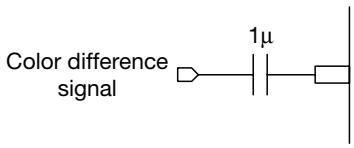
Input impedance: 8.6kΩ typ.</td></tr>
<tr><td>External circuit
 

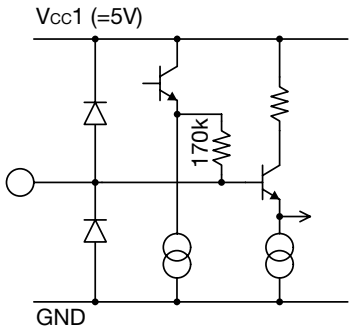
When not using it: open
Output signal</td><td>Equivalent circuit diagram
 
</td></tr>
</table>

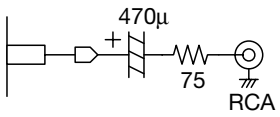
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">19</td><td rowspan="4">DAC YIN2</td><td>Function
Luminance signal (G-signal) input
Input clamp or bias select
Pin voltage: 1.1V typ. (Clamp select)
2.4V typ. (Bias select)
Input dynamic range: 1.3VP-P min.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

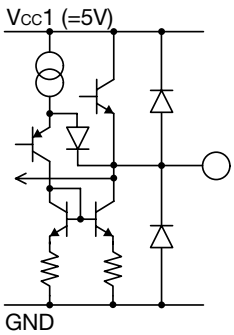
When not using it: open
Input signal
 
</td><td> 
</td></tr>
<tr><td rowspan="4">20</td><td rowspan="4">FSOUT</td><td>Function
DC output for SCART interface
It is the terminal which outputs Function switch signal of SCART interface.
The ternary output of L/M/H is controllable by I²C control. (refer to Switch Control Table)

Output impedance: 500Ω typ.
Low level output voltage: 0V typ.
Middle level output voltage: 6V typ.
High level output voltage: 10V typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td>When not using it: open
Output signal
DC voltage:
<table><tr><th>b01</th><th>b00</th><th colspan="2">DCOUT</th></tr><tr><td>0</td><td>0</td><td>L</td><td>Level 0</td></tr><tr><td>0</td><td>1</td><td>M</td><td>Level 1A</td></tr><tr><td>1</td><td>0</td><td rowspan="2">H</td><td rowspan="2">Level 1B</td></tr><tr><td>1</td><td>1</td></tr></table></td><td> 
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">21
22</td><td rowspan="2">DAC CbIN
DAC CrIN</td><td>
Function
Color difference signal input
Input bias
Pin voltage: 2.4V typ.
Input impedance: 170kΩ typ.
Input dynamic range: 1.3VP-P min.
External circuit


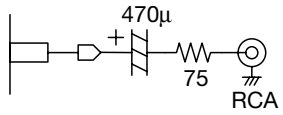
When not using it: open
Input signal
Color difference signal
0.7V
Equivalent circuit diagram


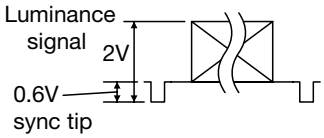
</td></tr>
<tr><td>
Function
Color difference output
It is a terminal for the Color difference signal external output.
Pin voltage: 2.4V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF
External circuit


When not using it: open
Output signal
Color difference signal
1.4V
Equivalent circuit diagram


</td></tr>
<tr><td>24
25</td><td>CrOUT
CbOUT</td><td></td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">26</td><td rowspan="4">YOUT2</td><td>Function
Luminance output (525p)
It is a terminal for a Luminance signal (525p) external output.

Pin voltage: 1.1V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF</td></tr>
<tr><td>External circuit
 

When not using it: open</td></tr>
<tr><td>Output signal
 
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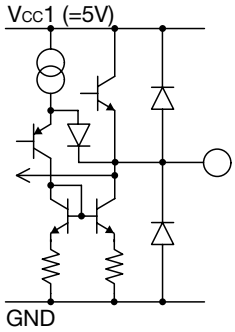
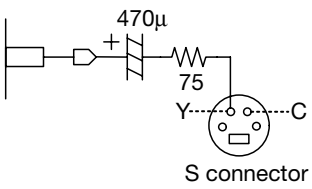
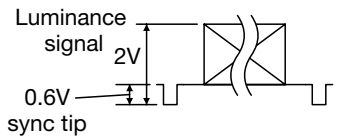
<tr><td>Equivalent circuit diagram
 
</td></tr>
<tr><td rowspan="4">27</td><td rowspan="4">YOUT1</td><td>Function
Luminance output (525i)
It is a terminal for a Luminance signal (525i) external output.

Pin voltage: 1.1V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF</td></tr>
<tr><td>External circuit
 

When not using it: open</td></tr>
<tr><td>Output signal
 
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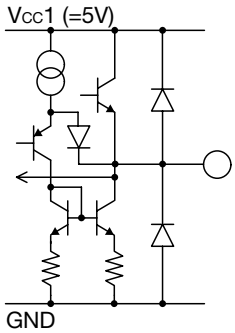
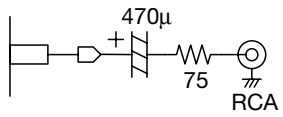
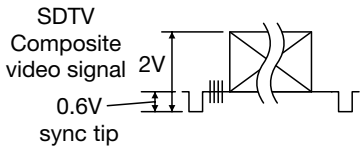
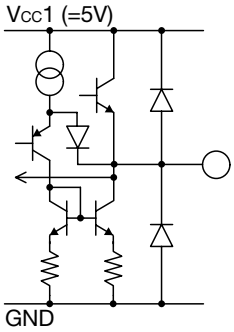
<tr><td>Equivalent circuit diagram
 
</td></tr>
</table>

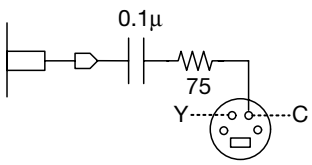
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>28
36
39</td><td>VOUT
VOUTAV2
VOUTAV1</td><td>
Function
Composite video output
It is a terminal for a composite video signal external output.

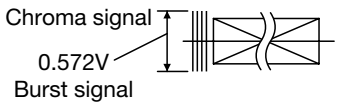
Pin voltage: 1.1V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF
External circuit


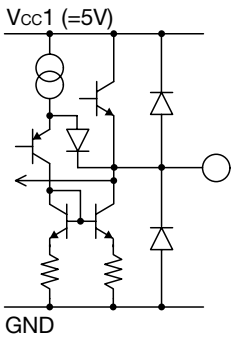
When not using it: open
Output signal


Equivalent circuit diagram


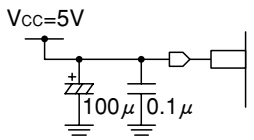
</td></tr>
<tr><td>29</td><td>COUT</td><td>
Function
Chroma output
It is a terminal for the Chroma signal external output.

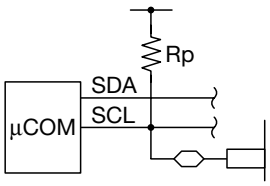
Pin voltage: 2.4V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF
External circuit


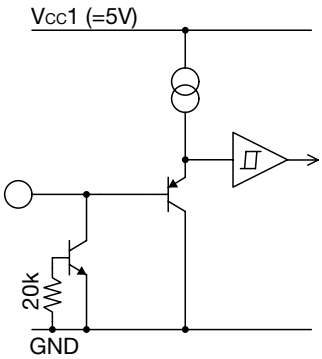
When not using it: open
Output signal


Equivalent circuit diagram


</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th colspan="2">Pin description</th></tr>
<tr><td rowspan="4">30</td><td rowspan="4">Vcc1</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Voltage supply
It is a supply voltage impression terminal. Please impress 5V.
Please arrange a bypass capacitor near the terminal.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

Input signal
DC voltage:
+4.5V~+5.5V</td><td></td></tr>
<tr><td rowspan="4">31</td><td rowspan="4">SCL</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Clock input of I²C BUS
It is the terminal which connects the SCL line of I²C BUS.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

Input signal
Input signal
Clock signal
 
</td><td> 
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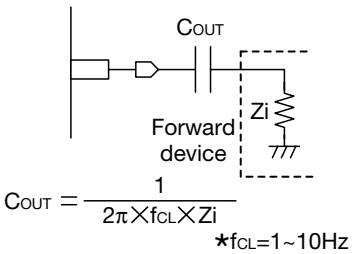
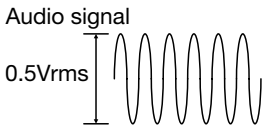
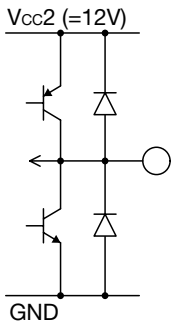
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">32</td><td rowspan="4">SDA</td><td>Function</td></tr>
<tr><td>DATA Input/Output of I²C BUS
It is the terminal which connects the SDA line of I²C BUS.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit: Rp, SDA, SCL, µCOM
Input output signal: Input signal — Control registers; Output signal — States registers; 1 2 6 7 8A 1 2 7 8A
Equivalent circuit diagram: Vcc1 (=5V), 20k, GND</td></tr>
<tr><td rowspan="5">34
35
37
38</td><td rowspan="5">RoutAV2
LoutAV2
RoutAV1
LoutAV1</td><td>Function</td></tr>
<tr><td>Audio signal output
It is a terminal for a audio signal external output.

Pin voltage: 6.3V typ.
Load resistance: 600Ω max.
Stray capacitance max.: 20pF</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit: Cout, Zi, Forward device
$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$ *fCL=1~10Hz
When not using it: open
Output signal: Audio signal, 0.5Vrms
Equivalent circuit diagram: Vcc5 (=12V), GND</td></tr>
</table>

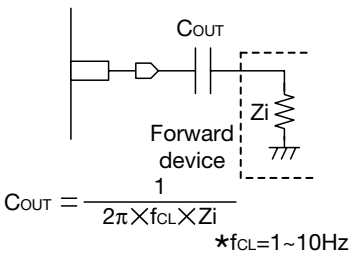
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>40
41</td><td>ROUTBUF
LOUTBUF</td><td>
Function
Audio signal output
It is a terminal for a audio signal output.

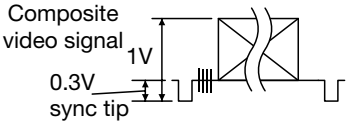
Pin voltage: 6.3V typ.
Load resistance: 1kΩ max.
Stray capacitance max.: 20pF
External circuit


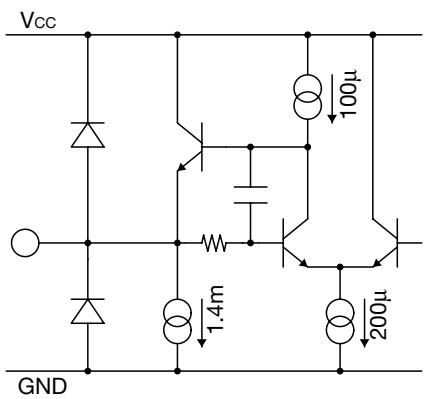
When not using it: open
Output signal


Equivalent circuit diagram


</td></tr>
<tr><td>42</td><td>VOUTBUF</td><td>
Function
Composite video output
It is a terminal for a composite video signal output.

Pin voltage: 1.1V typ.
Load resistance: 1kΩ max.
Stray capacitance max.: 20pF
External circuit


When not using it: open
Output signal


Equivalent circuit diagram


</td></tr>
</table>

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–55~+150	°C
Operating temperature	T_{OPR}	–20~+75	°C
Supply voltage	$V_{CC\ max.}$	13	V
Allowable loss (*1)	Pd	2.4	W

Note1: *1 Board mounting allowable loss. Board size: 190×150×1.6mm GE

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–20~+75	°C
Vcc1 Operating voltage	V_{CC1OP}	4.5~5.5	V
Vcc2 Operating voltage	V_{CC2OP}	11.2~12.8	V

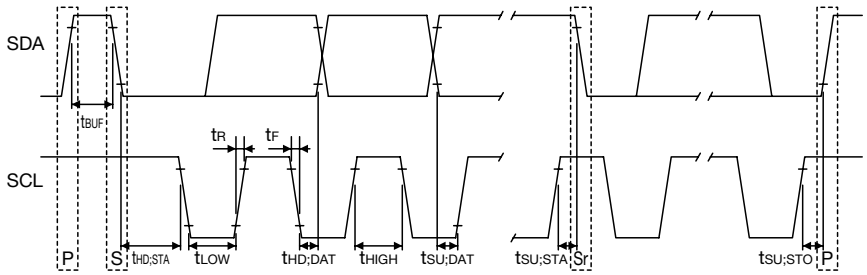
Electrical Characteristics (Except where noted otherwise Ta=25°C, V_{CC1}=5V, V_{CC2}=12V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Vcc1 supply current		I_{CC1}	No signal (V_{CC}=5V)	75	105	135	mA
Vcc2 supply current		I_{CC2}	No signal (V_{CC}=12V)	19	26	33	mA
Vcc1 supply current at standby		I_{CC3}	No signal (V_{CC}=5V)	18	25	32	mA
FSOUT Output voltage	H	FS_H	R_L=10kΩ	9.5	10.5	12	V
	M	FS_M		4.5	6	7	V
	L	FS_L		0	0.01	2	V
Terminal voltage	Video input (clamp)	V_{INCn}		0.8	1.1	1.4	V
	Video input (bias)	V_{INBn}		2.1	2.4	2.7	V
	Audio input	A_{INn}		6.5	7	7.5	V
	Video output (clamp)	V_{OUTCn}			1.1		V
	Video output (bias)	V_{OUTBn}			2.4		V
	Audio output	A_{OUTn}			6.3		V
[VOUTBUF]							
Voltage gain		G_{Vn}	SIN wave: 1V f=100kHz	–0.3	0	0.3	dB
Frequency characteristic		f_{Vn}	SIN wave: 1V 10MHz/100kHz	–1	0	1	dB
Output dynamic range		DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.9		V
Differential gain		DG_{Vn}	Staircase signal 1V		0.2	1	%
Differential phase		DP_{Vn}	Staircase signal 1V		0.1	1	deg
[VOUTAV1, VOUTAV2]							
Voltage gain		G_{Vn}	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic		f_{Vn}	SIN wave: 1V 6.75MHz/100kHz	–1	0	1	dB
Output dynamic range		DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain		DG_{Vn}	Staircase signal 1V		2	3	%
Differential phase		DP_{Vn}	Staircase signal 1V		1	2	deg

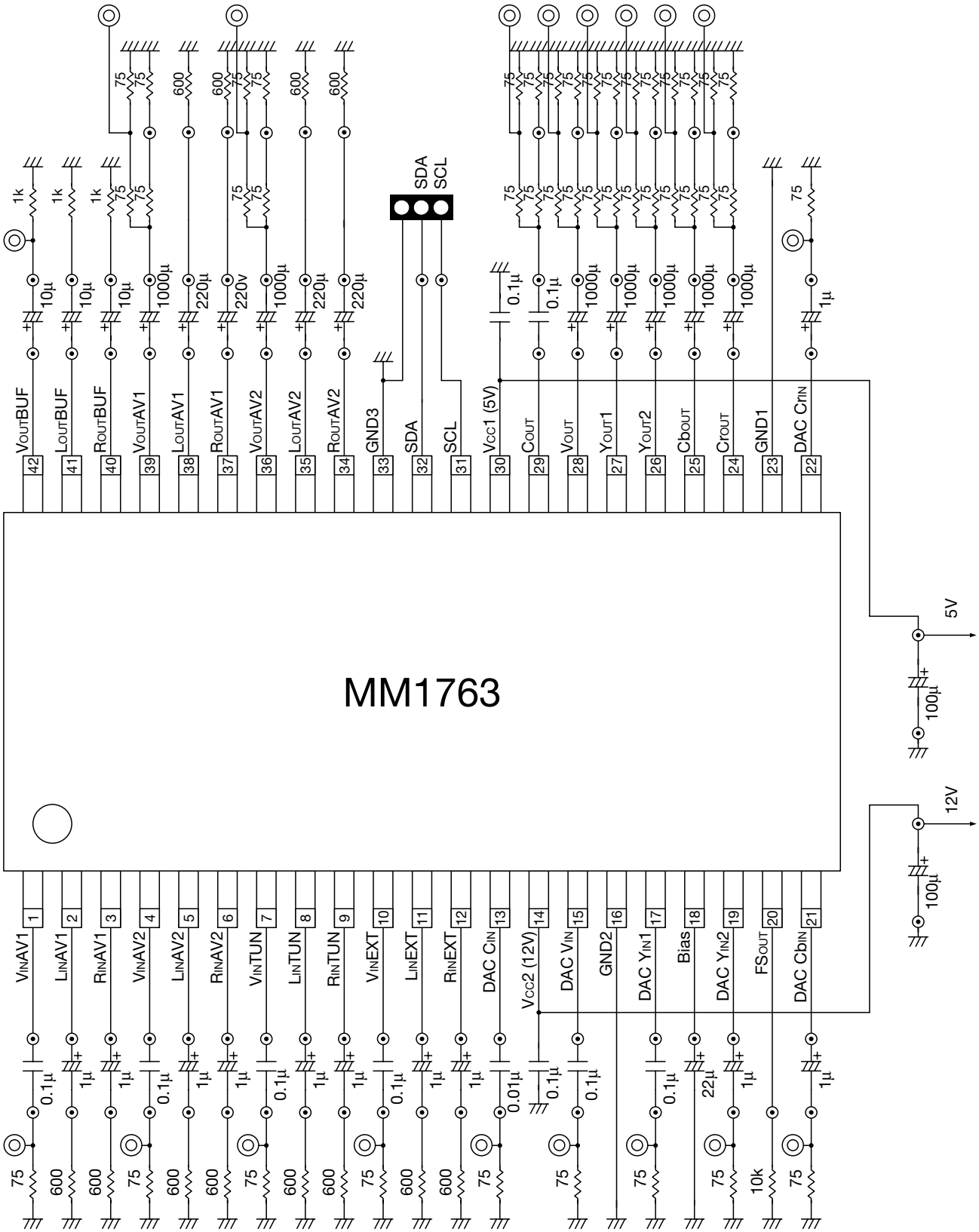
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[COUT, VOUT, YOUT1]						
Voltage gain	G_{Vn}	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1	$f1_{Vn}$	SIN wave: 1V 6.75MHz/100kHz	–1	0	1	dB
Frequency characteristic 2	$f2_{Vn}$	SIN wave: 1V 27MHz/100kHz		–30	–24	dB
Output dynamic range	DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain	DG_{Vn}	Staircase signal 1V		1	2	%
Differential phase	DP_{Vn}	Staircase signal 1V		1	2	deg
Signal/Noise	SN_{Vn}	BW: 100kHz~6MHz		80		dB
Group delay	t_{Vn}	at 100kHz		50	80	ns
Group delay deviation	Δt_{Vn}	to 3.58MHz		5	10	ns
		to 4.43MHz		10	20	ns
		to 6MHz		20	28	ns
[YOUT2, CbOUT, CrOUT]						
Voltage gain	G_{Vn}	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1	$f1_{V\ (YOUT2)}$	100 [IRE] SIN wave + 40 [IRE] sync 13.5MHz/100kHz	1 –	0	1	dB
Frequency characteristic 2	$f2_{VCbOUT, CrOUT}$	100 [IRE] SIN wave + 40 [IRE] sync 6.75MHz/100kHz	–1	0	1	dB
Frequency characteristic 3	$f3_{Vn}$	100 [IRE] SIN wave + 40 [IRE] sync 54MHz/100kHz		–30	–24	dB
Output dynamic range	DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain	DG_{Vn}	Staircase signal 1V		1	2	%
Differential phase	DP_{Vn}	Staircase signal 1V		1	2	deg
Signal/Noise	SN_{Vn}	BW: 100kHz~6MHz		80		dB
Group delay	t_{Vn}	at 100kHz		25	50	ns
Group delay deviation 1	$\Delta t1_{V\ (YOUT2)}$	to 2MHz		1	10	ns
		to 8MHz		2	10	ns
		to 12MHz		10	20	ns
Group delay deviation 2	$\Delta t2_{V\ (CbOUT)}$ $\Delta t2_{V\ (CrOUT)}$	to 1MHz		1	10	ns
		to 4MHz		2	10	ns
		to 6MHz		10	20	ns
[LOUTBUF, ROUTBUF]						
Voltage gain	$G0_{An}$	SIN wave: 1Vrms f=1kHz	–0.5	0	0.5	dB
	$G6_{An}$	SIN wave: 0.5Vrms f=1kHz	5.5	6	6.5	dB
Output dynamic range	DR_{An}	SIN wave: 1kHz THD=1%	3			Vrms
Total harmonic distortion	THD_{An}	SIN wave: 1kHz, 0dB VOUT=1Vrms, RL=10kΩ 30kHz–LPF		0.005	0.05	%
Output noise voltage	VN_{An}	A curve		3		μVrms
Output offset voltage	VOF_{An}	at the switching		0	±15	mV

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[LOUTAV1, LOUTAV2, ROUTAV1, ROUTAV2]							
Voltage gain		$G0_{An}$	SIN wave: 1Vrms f=1kHz	–0.5	0	0.5	dB
		$G2_{An}$	SIN wave: 0.79Vrms f=1kHz	1.5	2	2.5	dB
		$G4_{An}$	SIN wave: 0.63Vrms f=1kHz	3.5	4	4.5	dB
		$G6_{An}$	SIN wave: 0.5Vrms f=1kHz	5.5	6	6.5	dB
		$G8_{An}$	SIN wave: 0.4Vrms f=1kHz	7.5	8	8.5	dB
		$G10_{An}$	SIN wave: 0.32Vrms f=1kHz	9.5	10	10.5	dB
		$G12_{An}$	SIN wave: 0.25Vrms f=1kHz	11.5	12	12.5	dB
Output dynamic range		DR_{An}	SIN wave: 1kHz THD=1%	3			Vrms
Total harmonic distortion		THD_{An}	SIN wave: 1kHz, 0dB V_{OUT}=1Vrms, R_L=10kΩ 30kHz–LPF		0.005	0.05	%
Output noise voltage		VN_{An}	A curve		5		μVrms
Output offset voltage		VOF_{An}	at the switching		0	±15	mV
Crosstalk	VOUT	CTV_n			–60	–50	dB
	LOUT, ROUT	CT_{An}			–90	–70	dB
Video input impedance		Z_{inVn}	13, 21, 22 pin	120	170	220	kΩ
Audio input impedance		Z_{inAn}	L: 2, 5, 8, 11, R: 3, 6, 9, 12 pin	50	70	90	kΩ
Output impedance		Z_{OUT}	FS_{OUT}	300	500	800	Ω
Standby $V_{CC}2$ input voltage	L	$V_{THVCC2L}$				2.0	V
	H	$V_{THVCC2H}$		3.5			V
[I²C condition]							
Input voltage L		V_{IL}		0		0.7	V
Input voltage H		V_{IH}		2.1		5.0	V
SDA low level output voltage		V_{OL}	SDA sink 3mA	0		0.4	V
High level input current		I_{IH}	SDA, SCL=4.5V	–10		10	μA
Low level input current		I_{IL}	SDA, SCL=0.4V	–10		10	μA
Clock frequency		f_{SCL}				100	kHz
Data transfer wait time		t_{BUF}		4.7			μs
SCL start hold time		$t_{HD;STA}$		4.0			μs
SCL low level hold time		t_{LOW}		4.7			μs
SCL high level hold time		t_{HIGH}		4.0			μs
Start condition setup time		$t_{SU;STA}$		4.7			μs
SDA data hold time		$t_{HD;DAT}$		0			μs
SDA data setup time		$t_{SU;DAT}$		250			ns
SDA, SCL rise time		t_R				1000	ns
SDA, SCL fall time		t_F				300	ns
Stop condition setup time		$t_{SU;STO}$		4.0			μs

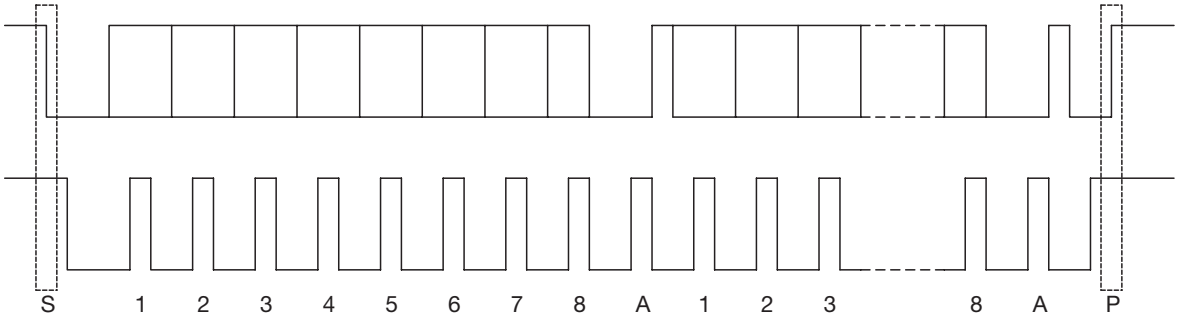
Note: I²C condition



Measuring Circuit



I²C BUS



I²C BUS is inter IC bus system controled by 2 lines (SDA, SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.

S	Slave address							R/W	A	DATA1								A
	1	0	0	1	0	0	0	0		b07	b06	b05	b04	b03	b02	b01	b00	

Address byte — Control data byte

DATA2								A	DATA3								A	P
b17	b16	b15	b14	b13	b12	b11	b10		b27	b26	b25	b24	b23	b22	b21	b20		

Control data byte

Out of the Address byte, first 7 bits are assigned to the slave address, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used as control register. MM1763 slave address is 90H.
The next figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

[Control data]

No.	Control DATA condition							
DATA1	b07	b06	b05	b04	b03	b02	b01	b00
	VOUTBUF select		VOUTAV1 select		VOUTAV2 select		FS CTRL	
DATA2	b17	b16	b15	b14	b13	b12	b11	b10
	L/ROUTBUF select		L/ROUTAV1 select		L/ROUTAV2 select			L/ROUTBUF mute
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	0, 6dB select	clamp bias sel	VOUT mute	L/ROUTAV1 gain select		L/ROUTAV2 gain select		

MM1763 consists of one address byte and three control data bytes (4bytes in total). All data over the limited length (5th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the separate table.

Switch Control Table

Control register 1 (2nd byte)

Control register 1								V_{OUT}BUF select	V_{OUT}AV1 select	V_{OUT}AV2 select	FS CTRL
b07	b06	b05	b04	b03	b02	b01	b00				
0	0							V_{IN}TUN			
0	1							V_{IN}AV1			
1	0							V_{IN}AV2			
1	1							V_{IN}EXT			
		0	0						V_{IN}AV2		
		0	1						V_{IN}TUN		
		1	0						V_{IN}EXT		
		1	1						DAC V_{IN}		
				0	0					V_{IN}AV1	
				0	1					V_{IN}TUN	
				1	0					V_{IN}EXT	
				1	1					DAC V_{IN}	
						0	0				Low
						0	1				Middle
						1	0				High
						1	1				High

Control register 2 (3rd byte)

Control register 2								L/R_{OUT}BUF select	L/R_{OUT}AV1 select	L/R_{OUT}AV2 select	L/R_{OUT}BUF mute
b17	b16	b15	b14	b13	b12	b11	b10				
0	0							L/R_{IN}TUN			
0	1							L/R_{IN}AV1			
1	0							L/R_{IN}AV2			
1	1							L/R_{IN}EXT			
		0	0						mute		
		0	1						L/R_{IN}TUN		
		1	0						L/R_{IN}AV2		
		1	1						L/R_{IN}EXT		
				0	0					mute	
				0	1					L/R_{IN}TUN	
				1	0					L/R_{IN}AV1	
				1	1					L/R_{IN}EXT	
							0				on
							1				off

Control register 3 (4th byte)

Control register 3								0/6dB select	clamp/bias select	VOUT mute CTRL	L/ROUTAV1 gain select	L/ROUTAV2 gain select
b27	b26	b25	b24	b23	b22	b21	b20					
0								0 dB				
1								6 dB				
	0								bias			
	1								clamp			
		0								active		
		1								mute		
			0	0							0 dB	
			0	1							2 dB	
			1	0							4 dB	
			1	1							6 dB	
					0	0						0 dB
					0	1						2 dB
					1	0						4 dB
					1	1						6 dB

[Status registers]

There is no preparation of the status register in MM1763. A status register returns all the 1 when 1 is set in the R/W bit.

At this time, the control of each switch is not done at all.

Application Circuit