National Semiconductor™

June 1996

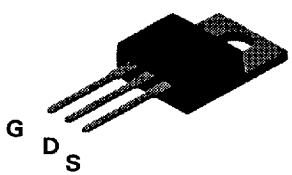
NDP6030L / NDB6030L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

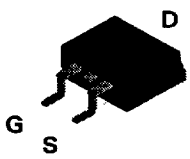
These N-Channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

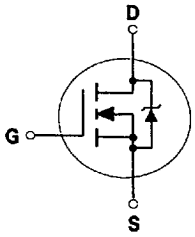
- 52 A, 30 V. $R_{DS(ON)}$ = 0.0135 Ω @ V_{GS}=10 V
  $R_{DS(ON)}$ = 0.020 Ω @ V_{GS}=4.5 V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low $R_{DS(ON)}$.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6030L	NDB6030L	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
I_D	Drain Current - Continuous	52		A
	- Pulsed	156		
P_D	Total Power Dissipation @ T_C = 25°C	75		W
	Derate above 25°C	0.5		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 52 A			100	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				52	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	µA
		T_J = -55°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	3	V
		T_J = 125°C	0.7	1	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 26 A		0.011	0.0135	Ω
		T_J = 125°C		0.017	0.024	
		V_{GS} = 4.5 V, I_D = 21 A		0.018	0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	15			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 26 A		32		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1350		pF
C_{oss}	Output Capacitance			800		pF
C_{rss}	Reverse Transfer Capacitance			300		pF

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 52A, V_{GS} = 10 V, R_{GEN} = 24Ω		8	16	nS
t_r	Turn - On Rise Time			130	250	nS
$t_{D(off)}$	Turn - Off Delay Time			45	90	nS
t_f	Turn - Off Fall Time			108	200	nS
Q_g	Total Gate Charge	V_{DS}= 10 V, I_D = 52 A, V_{GS} =10V		44	60	nC
Q_{gs}	Gate-Source Charge			6		nC
Q_{gd}	Gate-Drain Charge			14		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				52	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				120	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 26 A (Note 1)		0.93	1.3	V
		T_J = 125°C		0.85	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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Typical Electrical Characteristics

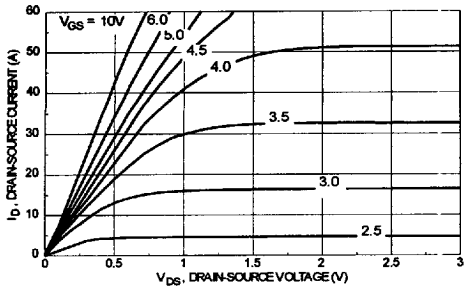

Figure 1. On-Region Characteristics

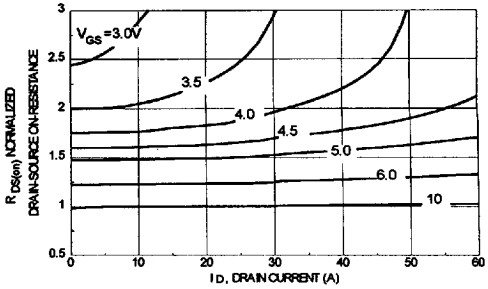

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

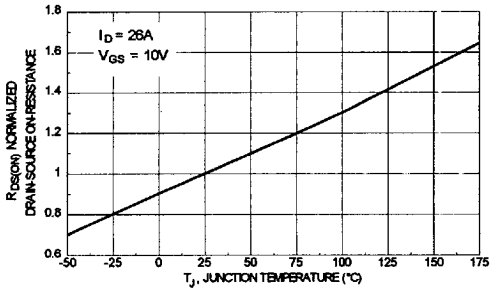

Figure 3. On-Resistance Variation with Temperature

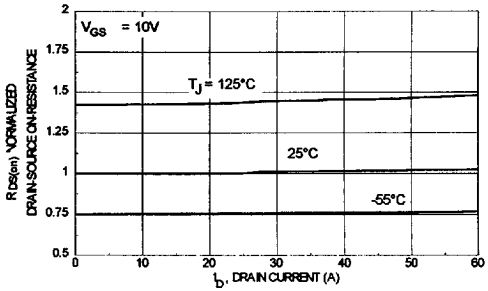

Figure 4. On-Resistance Variation with Drain Current and Temperature

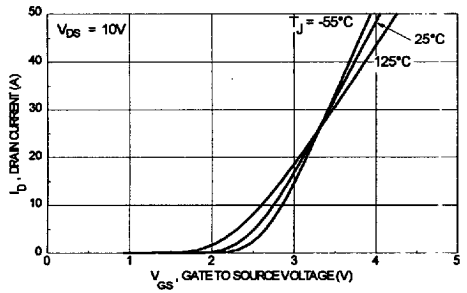

Figure 5. Transfer Characteristics

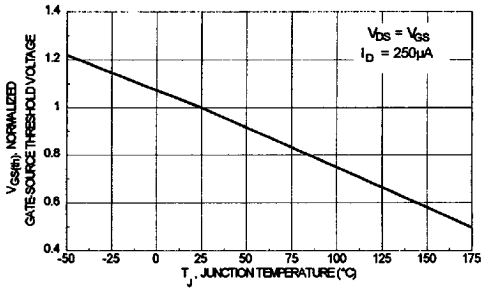

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

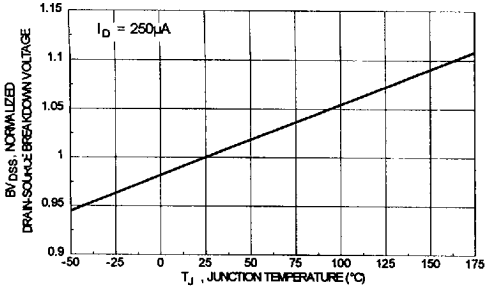

Figure 7. Breakdown Voltage Variation with Temperature

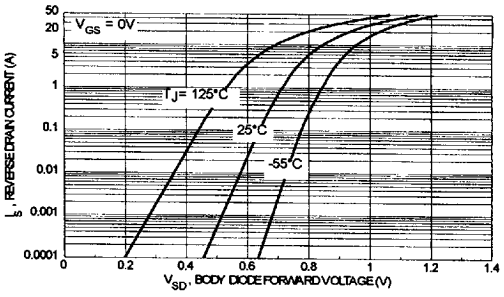

Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

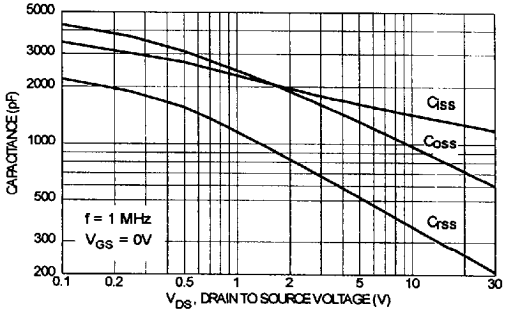

Figure 9. Capacitance Characteristics

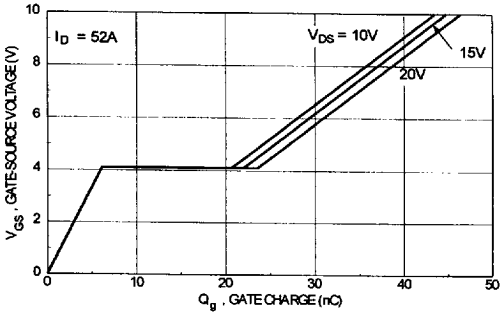

Figure 10. Gate Charge Characteristics

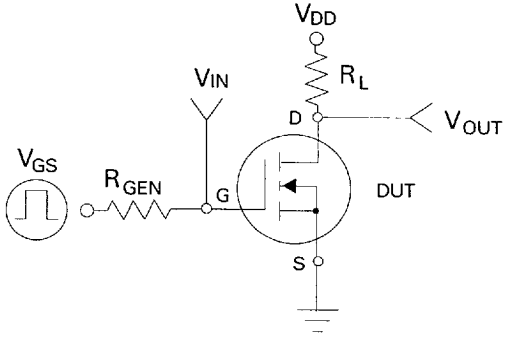

Figure 11. Switching Test Circuit

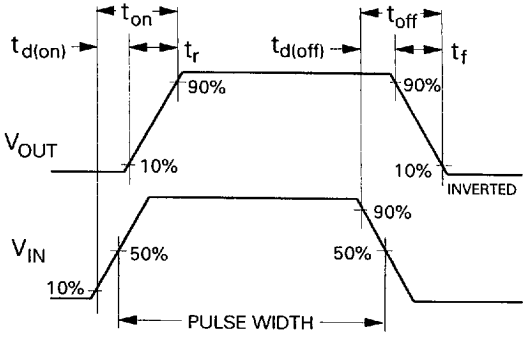

Figure 12. Switching Waveforms

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Typical Electrical Characteristics (continued)

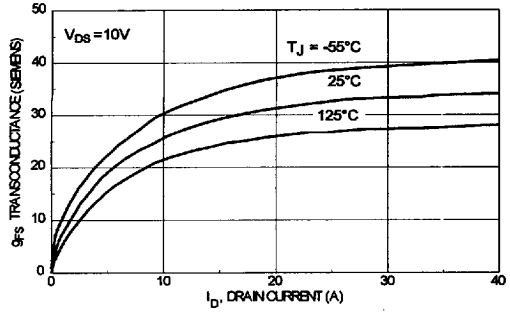

Figure 13. Transconductance Variation with Drain Current and Temperature

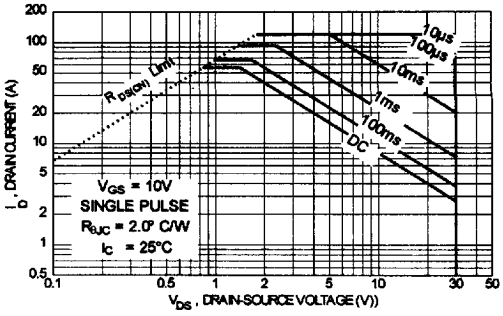

Figure 14. Maximum Safe Operating Area

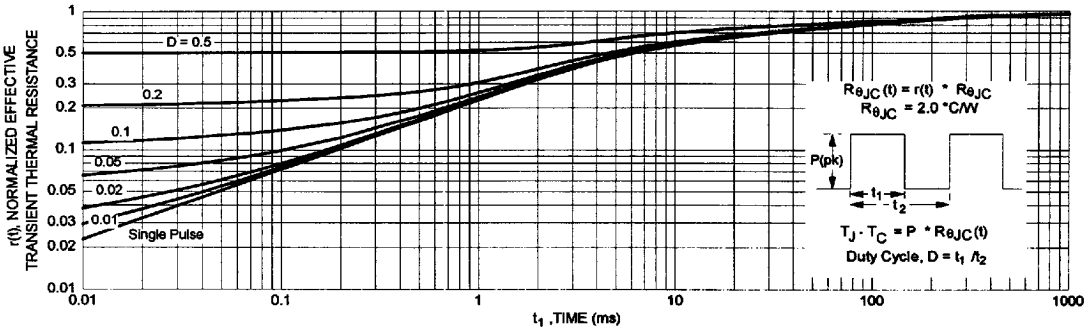

Figure 15. Transient Thermal Response Curve