PIC12F629/675

PIC12F629/675 Rev. A Silicon/Data Sheet Errata

The PIC12F629/675 parts you have received conform functionally to the Device Data Sheet (DS41190**C**), except for the anomalies described below.

All issues listed here will be addressed in future revisions of the **PIC12F629/675 silicon**.

1. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer interrupt service routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41190C), the following clarifications and corrections should be noted.

1. Module: GPIO Port

Register 3-2, “TRISIO – GPIO Tri-state Register (Address: 85h)”, is incorrect. Bits 5-4 and 2-0 should read “R/W-1”, as shown below:

REGISTER 3-2: TRISIO – GPIO TRI-STATE REGISTER (ADDRESS: 85h)

U-0	U-0	R/W-**1**	R/W-**1**	R-1	R/W-**1**	R/W-**1**	R/W-**1**
—	—	TRISIO5	TRISIO4	TRISIO3**(1)**	TRISIO2	TRISIO1	TRISIO0
bit 7							bit 0

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **TRISIO<5:0>:** General Purpose I/O Tri-State Control bit
1 = GPIO pin configured as an input (tri-stated)
0 = GPIO pin configured as an output

Note 1: TRISIO<3> always reads '1'.

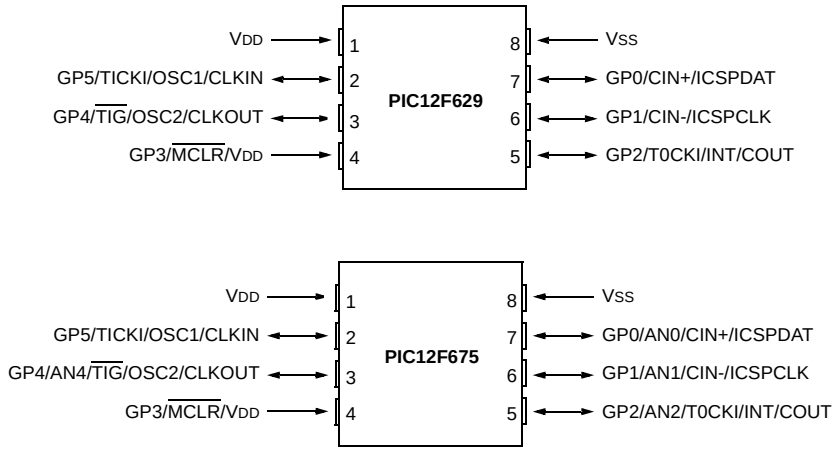
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2. Module: New 4x4 DFN Package Added

The new 8-pin 4x4 DFN pinout diagram will be added to the Pin Diagrams figure on page 2 and the Packaging Information chapter as shown below:

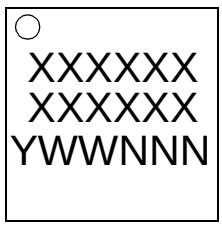
Pin Diagrams

8-pin DFN

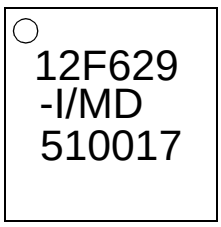


14.1 Package Marking Information

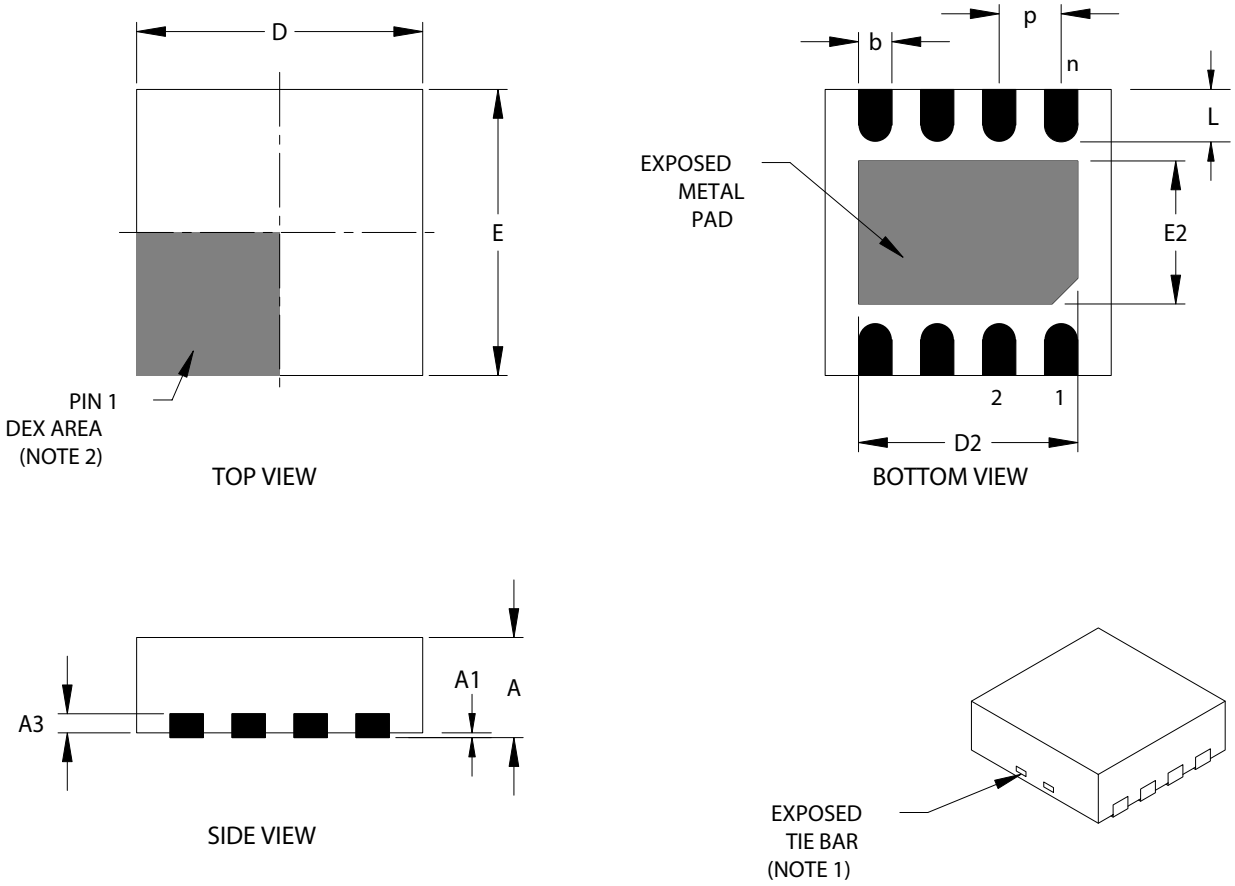
8-Lead DFN (4x4x1 mm)



Example



8-Lead Plastic Dual Flat No Lead Package (ML) 4x4x1 mm Body (DFN) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.031 BSC [5]			0.80 BSC [5]	
Overall Height	A	.029	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008 REF. [6]			0.20 REF. [6]	
Overall Length	E		.157 BSC [5]			4.00 BSC [5]	
Exposed Pad Width (Note 3)	E2	.100	.106	.112	2.55	2.70	2.85
Overall Width	D		.157 BSC [5]			4.00 BSC [5]	
Exposed Pad Length (Note 3)	D2	.132	.138	.144	3.35	3.50	3.65
Contact Width	b	.009	.012	.015	0.23	0.30	0.37
Contact Length	L	.008	.016	.020	0.20	0.40	0.50

*Controlling Parameter

Notes:

1. Package may have one or more exposed tie bars at ends.
2. Pin 1 visual index feature may vary, but must be located within the hatched area.

APPENDIX A: REVISION HISTORY

Rev. A Document (3/2002)

First revision of this document. Revised Table 12.3

Rev. B Document (9/2002)

Added Module 1: “In-Circuit Serial Programming™”, changes made to the Typical In-Circuit Serial Programming Connection, Figure 9-18.

Rev. C Document (04/02/04)

Removed Table 12.3 and Figure 9-18 due to Data Sheet revisions.
Added Module 1: “GPIO Port”, changes made to the TRISIO – GPIO Tri-state Register.

Rev. D Document (11/2004)

Added Module 1: “Data EEPROM Memory” for PIC12F629/675 silicon.

Rev. E Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 2: New 4x4 DFN Package added.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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