R96FE 9600 bps Facsimile Engine Device Set

INTRODUCTION

The R96FE FAXENGINE™ provides a complete set of facsimile machine control functions integrated into a 2-package VLSI device set. This integration reduces the manufacturer's hardware and development costs by eliminating external components. The device set consists of an Integrated Facsimile Controller (IFC) and a 9600 bps MONOFAX® modem.

The IFC performs the primary facsimile machine control and monitoring functions interfacing with the major fax machine components. Scanner, printer, and keyboard interfaces are included as are motor control drivers and the modem interface. These functions and interfaces are programmable to support a wide range of hardware peripherals. CCITT T.4 data compression/decompression functions (MH and MR) are implemented by the IFC. Fax machine video processing functions are provided utilizing an on-board flash A/D converter for up to 64 levels of gray scale. The IFC is supplied in an industry-standard 160-pin plastic quad flat package (PQFP).

The MONOFAX modem is a synchronous 9600 bps half-duplex modem (R96DFX or R96VFX) which offers connectivity and compatibility with fax machines world-wide.

An R96FE Development System can be purchased to reduce the manufacturer's design costs and time-to-market. The R96FE Development System includes:

1. The FAXENGINE Evaluation System (FEES): a stand-alone development board that acts as the fax machine motherboard. The FEES includes an IFC socket; ROM and RAM; LCD and keyboard/LED modules; speaker; phone jack; printer and scanner interfaces; and data access arrangement (DAA) circuitry. Video processing, modem, and DAA daughterboards are also included.

2. A FAXENGINE ROM Emulator (FERE): a personal computer-based code development aid with breakpoint and trace capability for debugging customer-created firmware that will operate in the R96FE external ROM.

3. A royalty free license to use the development software consisting of Rockwell's core macros (high-level routines common to fax machines) and core primitives (low-level routines for accessing FAXENGINE hardware) supplied in object code. An example application program for a typical complete fax machine is supplied in assembly source code. This example code, although not intended for production, can be used as a basis for developing a customer's specific fax machine application.

FEATURES

- Integrates facsimile control circuitry
  - —Reduces device count; saves board space
  - —Simplifies design; reduces production cost
  - —Reduces development time and cost
  - —Reduces power dissipation
- Facsimile processing firmware provided
  - —Reduces development time and cost
  - —Macros and primitives in object code
  - —Example application in assembly source code
- T.4 MH/MR compression/decompression in hardware
- Programmable thermal printer interface
  - —Up to 9 strobes
  - —On-chip thermal head temperature A/D converter
- Programmable scanner interface
  - —No external sample and hold required
  - —Scan widths to 2048 pixels (B4)
  - —5 ms minimum scan time
- Programmable control for two stepper motors
- Programmable operator panel interface
  - —32 keys, 8 LEDs, one LCD module
- Programmable tone output for operator alert
- Video processing
  - —6-bit flash A/D converter with voltage reference inputs supports external background correction
  - —Scanner shading correction (8 bits/pixel)
    - 1 correction per 8 pixels with internal RAM
    - 1 correction per pixel with external RAM
  - —Configurable dither table (up to an 8 x 8 pattern)
- Internal MC19 CPU
  - —7 MHz clock speed
  - —Programmable wait states for external devices
- 26 to 34 general purpose input/output (GPIO) pins

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HARDWARE DESCRIPTION

The R96FE FAXENGINE general hardware interface is illustrated in Figure 1.

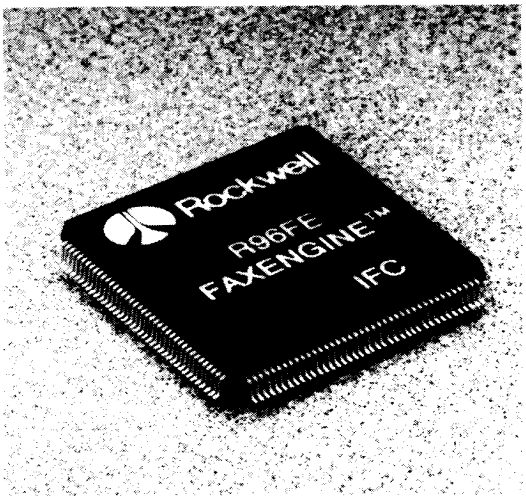
Integrated Facsimile Controller (IFC)

The IFC contains an internal 8-bit microprocessor and dedicated circuitry optimized for facsimile signal processing and facsimile machine control and monitoring.

Microprocessor. The microprocessor is an enhanced MC19 central processing unit (CPU). This CPU provides fast instruction execution and memory efficient input/output bit manipulation. The CPU connects to other internal IFC functions over a 16-bit address/8-bit data bus and dedicated control lines. The bus is routed outside the IFC for external memory access.

Scanner, Printer Motor Control. Eight outputs are provided to external current drivers; four for the scanner motor and four for the printer motor. Firmware primitives support up to a 256-step control pattern for each motor.

Expansion Bus Control. Address, data, control, status, and decoded chip select signals support connection to external ROM, optional RAM, and optional peripheral devices.



R96FE FAXENGINE Integrated Facsimile Controller (IFC)

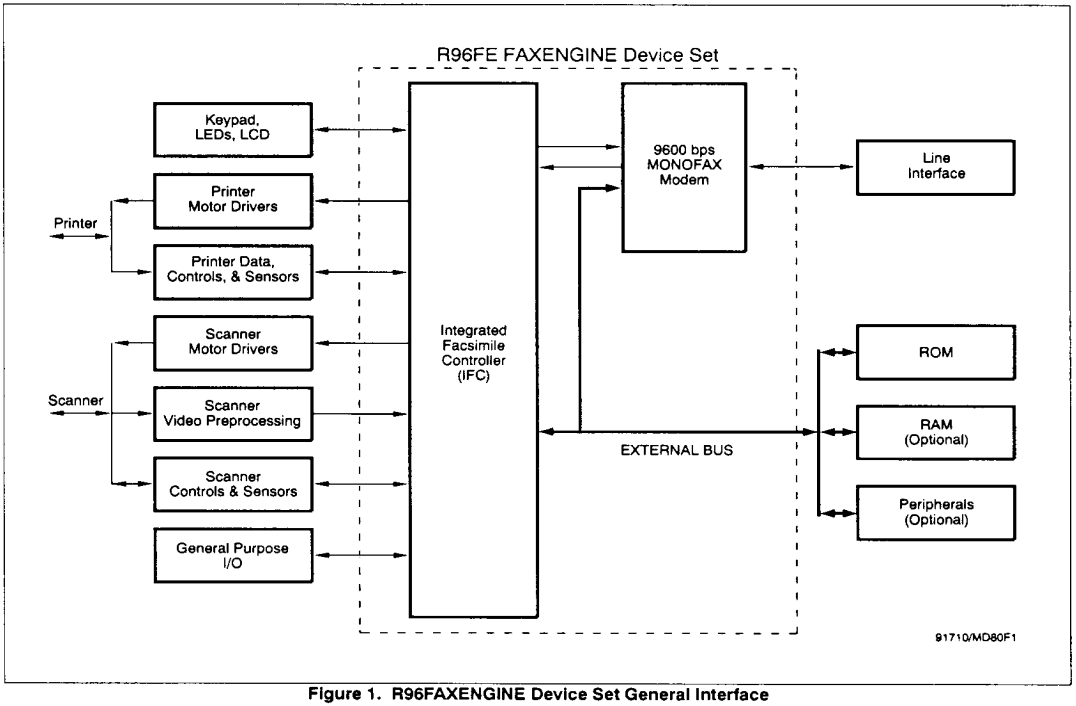


Figure 1. R96FAXENGINE Device Set General Interface

Operator Interface. Four enable inputs, eight strobe outputs, and two control outputs support the operator interface. A 32-key keypad can be supported directly. An 8 x 15 keyboard (120 keys) can be supported with external circuitry.

The strobe outputs can also be used as LED drivers or as LCD data lines. Up to eight LEDs can be directly driven.

A wide variety of LCD displays can be driven using a 4-bit data bus and two separate control lines.

Video Control. Seven programmable control and timing signals support common CCD and CIS scanners. The video control function provides signals for controlling the scanner and for processing its video output.

Scanner Flash A/D Converter. A 6-bit flash A/D converter interfaces to the scanner. The A/D reference inputs are made available for control by external background correction circuits.

T.4 Compressor/Decompressor. IFC hardware provides MH and MR data compression and decompression per CCITT Recommendation T.4.

Video Processing. The IFC provides shading RAM and support firmware for two modes of correction for scanner non-linearities arising from uneven sensor output or uneven illumination. In one mode, correction is provided on an 8-pixel group at a time basis; 256 bytes of IFC internal RAM store one byte of correction for each eight consecutive pixel positions. In the other mode, correction is applied separately to each pixel; 2K bytes of internal RAM are used. When using the one correction byte per pixel mode, external RAM is required to store CPU variables.

The IFC includes a dither table ranging in size up to 8 x 8; rows and columns are independent. The dither table is stored in internal RAM (8 bits per element).

External ROM. External ROM stores all the FAXENGINE program object code.

MONOFAX Modem

The modem is a synchronous 9600 bps half-duplex R96DFX or R96VFX MONOFAX modem. These modems support Group 3 fax, HDLC framing, tone generation, and DTMF reception in the R96FE application. The R96VFX also provides a voice coder/decoder. The modem can operate over the public switched telephone network (PSTN) or the general switched telephone network (GSTN) through line terminations provided by a data access arrangement (DAA). The modem satisfies the requirements specified by CCITT recommendations V.29, V.27 ter, V.21 Channel 2, and T.4, and meets the binary signaling requirements of T.30. The modem can operate at 9600, 7200, 4800, 2400, or 300 bps, and also includes the V.27 short training sequence option.

HARDWARE INTERFACE DESCRIPTION

Scanner Interface

Video A/D Converter

Accuracy: ± 0.5 LSB
Input range: 0 to VDD
Vref differential input range: 0.8 V to 3.0 V
Operating range: –VREF to +VREF
No sample and hold circuit required

Scanner Control

Four output signals: START, CLK1, /CLK1, CLK2
Scan line period: 4 to 40 ms
Dot sample point: Programmable to 1/16 dot period
Control signal rising and falling edges:
Independently programmable to 1/16 dot period

Video Circuitry Control

Three output signals: VIDCTL0, VIDCTL1, VIDCTL2
VIDCTL0 rising and falling edges:
Independently programmable within each dot period
VIDCTL1 and VIDCTL2 rising and falling edges:
Independently programmable within a scan line period

Scan Data Transfer Control (VIDCTL2)

Scan start delay: 0 to 2047 dots
Line length: 8 to 2048 dots, modulo 8

Video Processing

Dither table: Programmable to an 8 x 8 pattern
Independent rows and columns
Shading correction: Up to 50% ADC range

Printer Interface

Print Data Transfer Control

Three output signals: PDAT, PCLK, PLAT
Polarity control: Programmable on all three outputs
Line period: 4 to 40 ms
Data offset: 0 to 2040 dots, modulo 8
Number of dots: 8 to 2048 dots, modulo 8

Strobe Generation

Strobe count: 1 to 9 strobes
Polarity control: Strappable
Prescaler clock: 1 to 8 printer data clocks (PCLK)
Strobe period: 1 to 256 prescaler clocks
Strobe width: 1 to 256 prescaler clocks
Strobe width adjustable at the start of each line
Non-overlapping strobes

Temperature A/D Conversion

Resolution: 8 bits

Accuracy: 6 bits

Conversion time: Less than 2 ms

Power-On Reset (/PORES) Input

/PORES input initializes R96FE upon power turn on.

Requires only a simple RC input network.

Reset (/RESET) Input/Output

Open drain input/output: Can accept external reset input or provide reset output to external circuit.

Watchdog Timer

IFC watchdog timer serviced by the IFC.

Programmable watchdog enable.

Programmable time-out period before reset.

Tone Generator

Single tone output

Programmable frequency: 20 to 4000 Hz

General Purpose I/O (GPIO)

26 GPIO signals (GPIO0 – GPIO10, HIO0 – HIO13, HIO15)

Unused printer strobes (PIO0 – PIO7)

Programmable direction control for all GPIO functions

System Timing

Timing source: External oscillator or modem clock

Two internal timer interrupts: 2 ms and 1/8 line time

External RAM Interface

Wait states for RAM chip select: 0 to 3

RAM access time: 70 ns with 0 wait states

External ROM Interface

Wait states for ROM chip select: 0 to 3

ROM access time: 70 ns with 0 wait states

POWER AND ENVIRONMENTAL REQUIREMENTS

R96FE power requirements are shown in Table 1.

R96FE environmental specifications are listed in Table 2.

REFERENCE DOCUMENTATION

Document	Order No.
R96DFX Modem Data Sheet	MD60
R96VFX Modem Data Sheet	MD77
R96FE FAXENGINE Development System Data Sheet	862
R96FE FAXENGINE Evaluation System Developer's Guide	864
R96FE FAXENGINE ROM Emulator User's Manual	865
9600 MONOFAX Modem Designer's Guide	820
MC19 Megacell CPU Programming Manual	413

HARDWARE INTERFACE SIGNALS

The R96FE functional hardware interface signals are shown in Figure 2.

IFC INTERFACE SIGNALS

The IFC hardware signal pin assignments are shown in Figure 3. The definitions of the pin signals are summarized in Table 3. The hardware signal characteristics are described in Table 4.

MONOFAX MODEM INTERFACE SIGNALS

The modem pin assignments are shown in Figure 4. The pin assignments are listed by pin number in Table 5.

The modem hardware interconnect signals are listed by functional group in Table 6.

Table 1. Power Requirements

Device	Voltage	Typ. Current @ 25°C	Max. Current @ 0°C
IFC	+5 VDC ±5%		
VDD & ADVD		75 mA	
ADVA		12 mA	
TADV		1 mA	
R96DFX	+5 VDC ±5%	60 mA	64 mA
	–5 VDC ±5%	14 mA	16 mA
R96VFX	+5 VDC ±5%	66 mA	70 mA
	–5 VDC ±5%	14 mA	16 mA

Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 microvolts peak.

Table 2. Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32°F to 158°F)
Storage	–40°C to 80°C (–40°F to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

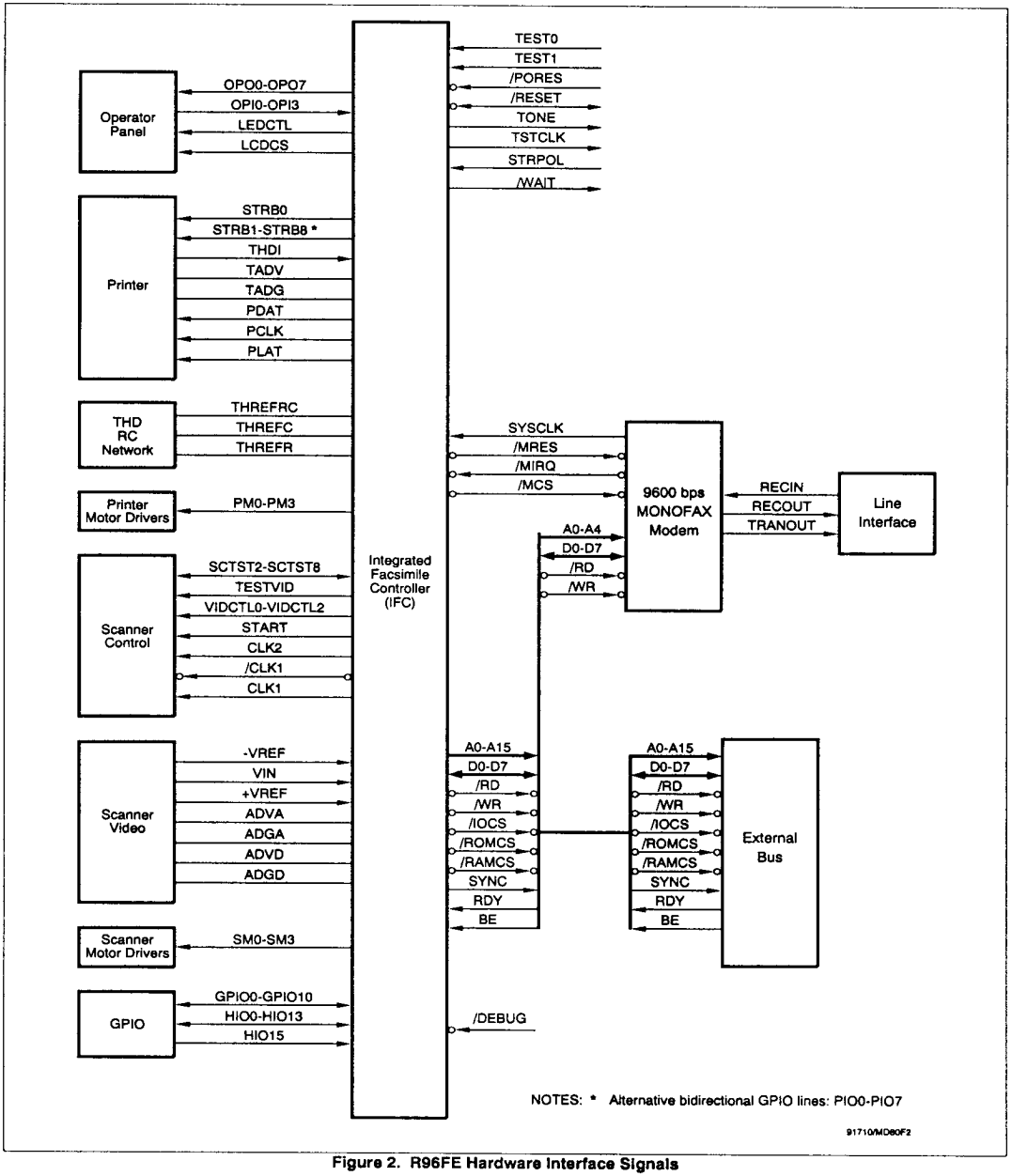


Figure 2. R96FE Hardware Interface Signals

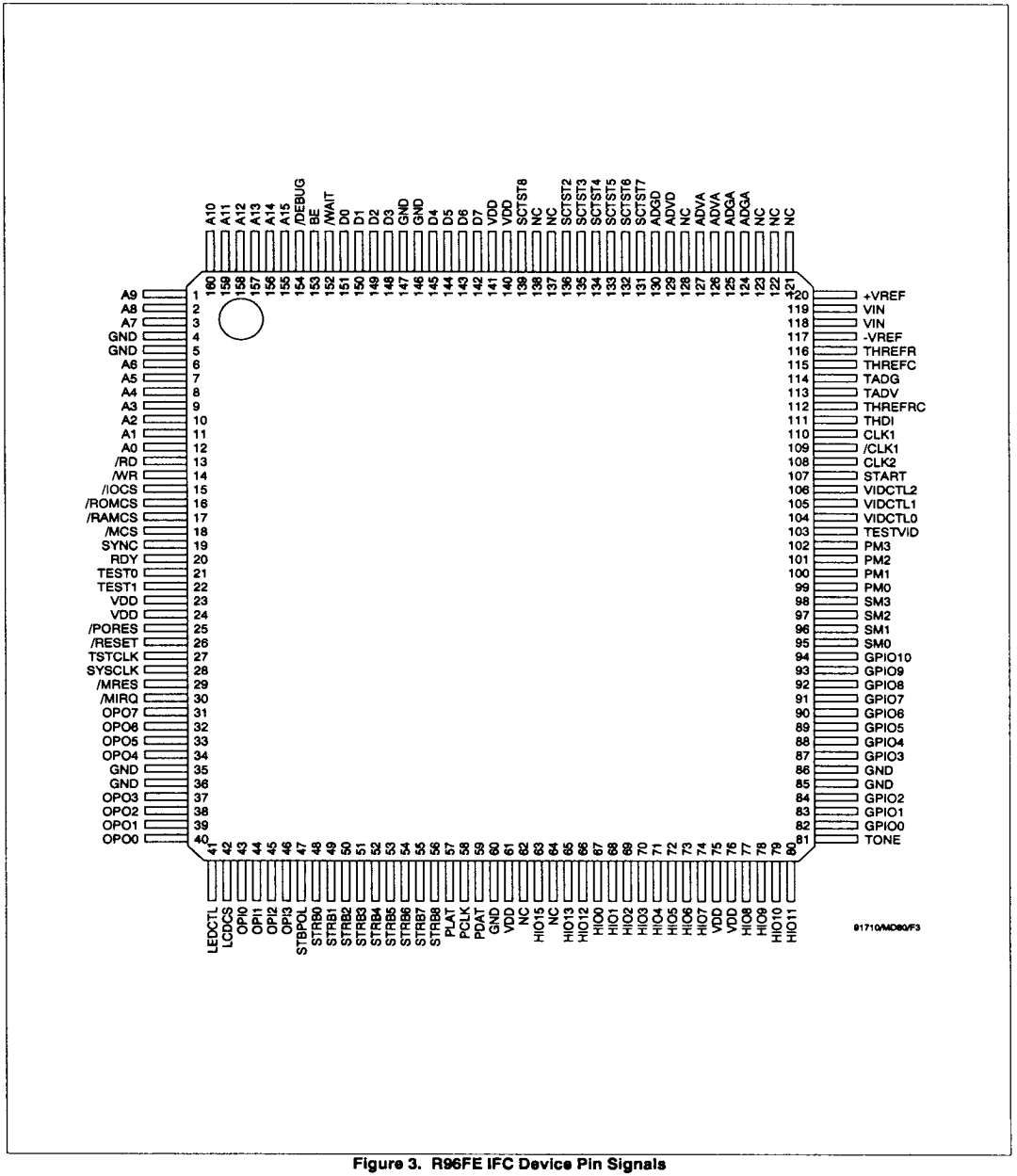


Figure 3. R96FE IFC Device Pin Signals

Table 3. R96FE IFC Pin Functions

Pin No.	Name	I/O	Description	Comments	Input Type	Output Type
System Bus Interface Signals						
1	A9	O	System Bus Address Line 9			2XT
2	A8	O	System Bus Address Line 8			2XT
3	A7	O	System Bus Address Line 7			2XT
4	GND		Ground	GND		
5	GND		Ground	GND		
6	A6	O	System Bus Address Line 6			2XT
7	A5	O	System Bus Address Line 5			2XT
8	A4	O	System Bus Address Line 4			2XT
9	A3	O	System Bus Address Line 3			2XT
10	A2	O	System Bus Address Line 2			2XT
11	A1	O	System Bus Address Line 1			2XT
12	A0	O	System Bus Address Line 0			2XT
13	/RD	O	System Bus Read Strobe			3XT
14	/WR	O	System Bus Write Strobe			3XT
15	/IOCS	O	System Bus I/O Chip Select			2XT
16	/ROMCS	O	System Bus ROM Chip Select			2XT
17	/RAMCS	O	System Bus RAM Chip Select			2XT
18	/MCS	O	Modem Chip Select			2XC
19	SYNC	O	CPU Opcode Read			2XT
20	RDY	I	CPU Wait State Control	Internal Pullup	TU	
21	TEST0	I	Test Control	Connect to GND	C	
22	TEST1	I	Test Control	Connect to GND	C	
23	VDD		Power (+5V)	VDD		
24	VDD		Power (+5V)	VDD		
Reset Signals						
25	/PORES	I	Power On Reset		H	
26	/RESET	I/O	Reset Host and FE	Int. Pullup, Hyst. In, Open Dr.	HU	2XC
System Clocks						
27	TSTCLK	O	Test Clock			3XC
28	SYSCLK	I	System Clock		CLKI	
Modem Interface						
29	/MRES	O	Modem Reset			2XC
30	/MIRQ	I	Modem Interrupt Request	Internal Pullup	CU	
Operator Panel Signals						
31	OPO7	O	KB/LED/LCD Strobe 7			2XL
32	OPO6	O	KB/LED/LCD Strobe 6			2XL
33	OPO5	O	KB/LED/LCD Strobe 5			2XL
34	OPO4	O	KB/LED/LCD Strobe 4			2XL
35	GND		Ground	GND		
36	GND		Ground	GND		
37	OPO3	O	KB/LED/LCD Strobe 3			2XL
38	OPO2	O	KB/LED/LCD Strobe 2			2XL
39	OPO1	O	KB/LED/LCD Strobe 1			2XL
40	OPO0	O	KB/LED/LCD Strobe 0			2XL
41	LEDCTL	O	LED Control			5XC
42	LCDCS	O	LCD Chip Select			1XC
43	OPI0	I	Keyboard Return 0	Pullup, Hysteresis In	HU	
44	OPI1	I	Keyboard Return 1	Pullup, Hysteresis In	HU	
45	OPI2	I	Keyboard Return 2	Pullup, Hysteresis In	HU	
46	OPI3	I	Keyboard Return 3	Pullup, Hysteresis In	HU	
Printer Strobes/GPIO (PIO)						
47	STBPOL	I	PTR Strobe Polarity		C	
48	STRB0	O	PTR Strobe			1XP
49	STRB1	I/O	PTR Strobe 1 or PIO0		H	1XP
50	STRB2	I/O	PTR Strobe 2 or PIO1		H	1XP
51	STRB3	I/O	PTR Strobe 3 or PIO2		H	1XP
52	STRB4	I/O	PTR Strobe 4 or PIO3		H	1XP
53	STRB5	I/O	PTR Strobe 5 or PIO4		H	1XP
54	STRB6	I/O	PTR Strobe 6 or PIO5		H	1XP
55	STRB7	I/O	PTR Strobe 7 or PIO6		H	1XP
56	STRB8	I/O	PTR Strobe 8 or PIO7		H	1XP

Table 3. R96FE IFC Pin Functions (Cont'd)

Pin No.	Name	I/O	Description	Comments	Input Type	Output Type
Printer Data Strobes						
57	PLAT	O	Printer Data Strobe			3XP
58	PCLK	O	Printer Clock			3XP
59	PDAT	O	Printer Data			2XP
60	GND		Ground	GND		
61	VDD		Power (+5V)	VDD		
Gereral Purpose I/O (HIO)						
62	NC		No Connection			
63	HIO15	I/O	HIO 15	Pullup	HU	2XC
64	NC		No Connection			
65	HIO13	I/O	HIO 13 or SCTST1	Pullup	HU	1XC
66	HIO12	I/O	HIO 12 or SCTST0	Pullup	HU	1XC
67	HIO0	I/O	HIO 0		H	2XC
68	HIO1	I/O	HIO 1		H	2XC
69	HIO2	I/O	HIO 2		H	2XC
70	HIO3	I/O	HIO 3		H	2XC
71	HIO4	I/O	HIO 4		H	2XC
72	HIO5	I/O	HIO 5		H	2XC
73	HIO6	I/O	HIO 6		H	2XC
74	HIO7	I/O	HIO 7		H	2XC
75	VDD		Power (+5V)	VDD		
76	VDD		Power (+5V)	VDD		
77	HIO8	I/O	HIO 8	Pullup	HU	1XC
78	HIO9	I/O	HIO 9	Pullup	HU	1XC
79	HIO10	I/O	HIO 10	Pullup	HU	1XC
80	HIO11	I/O	HIO 11	Pullup	HU	1XC
Tone Generator						
81	TONE	O	Tone Generator			1XC
Gereral Purpose I/O (GPIO)						
82	GPIO0	I/O	GPIO 0	Hysteresis In	H	1XC
83	GPIO1	I/O	GPIO 1	Hysteresis In	H	1XC
84	GPIO2	I/O	GPIO 2	Hysteresis In	H	1XC
85	GND		Ground	GND		
86	GND		Ground	GND		
87	GPIO3	I/O	GPIO 3	Hysteresis In	H	1XC
88	GPIO4	I/O	GPIO 4	Hysteresis In	H	1XC
89	GPIO5	I/O	GPIO 5	Hysteresis In	H	1XC
90	GPIO6	I/O	GPIO 6	Hysteresis In	H	1XC
91	GPIO7	I/O	GPIO 7	Hysteresis In	H	1XC
92	GPIO8	I/O	GPIO 8	Hysteresis In	H	1XC
93	GPIO9	I/O	GPIO 9 & IRQ8	Hysteresis In	H	1XC
94	GPIO10	I/O	GPIO 10 & /IRQ7	Hysteresis In	H	1XC
Motor Control Signals						
95	SM0	O	Scan Motor Phase 0			1XC
96	SM1	O	Scan Motor Phase 1			1XC
97	SM2	O	Scan Motor Phase 2			1XC
98	SM3	O	Scan Motor Phase 3			1XC
99	PM0	O	Print Motor Phase 0			1XC
100	PM1	O	Print Motor Phase 1			1XC
101	PM2	O	Print Motor Phase 2			1XC
102	PM3	O	Print Motor Phase 3			1XC
Scanner Control Signals						
103	TESTVID	O	Test Video			2XC
104	VIDCTL0	O	Video Control 0			2XC
105	VIDCTL1	O	Video Control 1			1XC
106	VIDCTL2	O	Video Control 2			1XC
107	START	O	Scanner Start			2XS
108	CLK2	O	Clock 2			2XS
109	/CLK1	O	Inverse Clock 1			2XS
110	CLK1	O	Clock 1			2XS

Table 3. R96FE IFC Pin Functions (Cont'd)

Pin No.	Name	I/O	Description	Comments	Input Type	Output Type
Theramal Head (THD) Sensor & Vref						
111	THDI	I	A/D Input		TA	
112	THREFRC		Resistor/Capacitor for THD Reference			
113	TADV		A/D Analog Power (+5V)		TADV	
114	TADG		A/D Analog GND		TADG	
115	THREFC		Capacitor for THD Reference			
116	THREFR		Resistor for THD Reference			
Scanner Video A/D Signals						
117	–VREF	I	A/D Reference Voltage (Neg.)		–VR	
118	VIN	I	Analog Video Input		VA	
119	VIN	I	Analog Video Input		VA	
120	+VREF	I	A/D Reference Voltage (Pos.)		+VR	
121	NC		No Connection	Connect to ADGA		
122	NC		No Connection	Connect to ADGA		
123	NC		No Connection	Connect to ADGA		
124	ADGA		A/D Analog Ground		VADG	
125	ADGA		A/D Analog Ground		VADG	
126	ADVA		A/D Analog Power (+5V)		VADV	
127	ADVA		A/D Analog Power (+5V)		VADV	
128	NC		No Connection	No Ext. connect		
129	ADVD		A/D Digital Power (+5V)		VADV	
130	ADGD		A/D Digital Ground		VADG	
Test Signals						
131	SCTST7	I	Test Control/ADUF	Pullup	CU	
132	SCTST6	I	Test Control/ADOF	Pullup	CU	
133	SCTST5	I	Test Control/ADD5	Pullup	CU	
134	SCTST4	I	Test Control/ADD4	Pullup	CU	
135	SCTST3	I	Test Control/ADD3	Pullup	CU	
136	SCTST2	I	Test Control/ADD2	Pullup	CU	
137	NC		No Connection			
138	NC		No Connection			
139	SCTST8	O	ADCLK			2XC
System Bus Interface Signals						
140	VDD		Power (+5V)	VDD		
141	VDD		Power (+5V)	VDD		
142	D7	I/O	System Bus Data Line 7		T	2XT
143	D6	I/O	System Bus Data Line 6		T	2XT
144	D5	I/O	System Bus Data Line 5		T	2XT
145	D4	I/O	System Bus Data Line 4		T	2XT
146	GND		Ground	GND		
147	GND		Ground	GND		
148	D3	I/O	System Bus Data Line 3		T	2XT
149	D2	I/O	System Bus Data Line 2		T	2XT
150	D1	I/O	System Bus Data Line 1		T	2XT
151	D0	I/O	System Bus Data Line 0		T	2XT
152	/WAIT	O	Wait State Indicator			2XT
153	BE	I	System Bus Enable	Pullup	TU	
154	/DEBUG	I	CPU NMI (Reserved)	Pullup	TU	
155	A15	O	System Bus Address Line 15			2XT
156	A14	O	System Bus Address Line 14			2XT
157	A13	O	System Bus Address Line 13			2XT
158	A12	O	System Bus Address Line 12			2XT
159	A11	O	System Bus Address Line 11			2XT
160	A10	O	System Bus Address Line 10			2XT

Notes: 1. **Name:** Identifies the pin's active polarity:
with / Active low
without / Active high or programmable polarity
2. **I/O:** Depicts the pin's input/output capability:
I Input only
O Output only
I/O Both Input and output

Table 4. R96FE IFC Hardware Signal Characteristics

Input Signal Characteristics

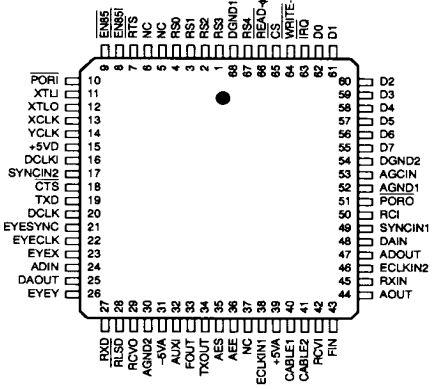
Input Type	Description	VIL (V max)	VIH (V min)	Hysterisis (V min)	Pullup Resistance (K ohm)
CLKI	Clock Input	0.3*VDD	0.7*VDD	--	--
C	CMOS Input	0.3*VDD	0.7*VDD	--	--
CU	CMOS/Pullup	0.3*VDD	0.7*VDD	--	35–150
CT	CMOS/Test	0.3*VDD	0.7*VDD	--	--
H	Hysteresis	0.25*VDD	0.7*VDD	0.9	--
HU	Hysteresis/Pullup	0.25*VDD	0.7*VDD	0.9	35–150
T	TTL Input	0.8	2.0	--	--
TU	TTL/Pullup	0.8	2.0	--	35–150

Absolute Input Range = –0.5 to VDD+0.5

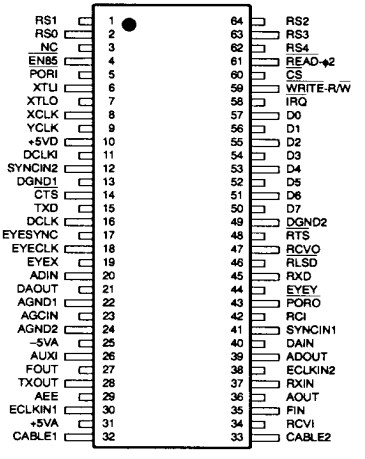
Input Type	Description	Operating (V min)	Operating (V max)	Absolute Max (V min)	Absolute Max (V max)
VA	Video Analog In	–VR	+VR	–0.5	VADV+0.5
TA	Thermal Head Analog In	0	VDD/2	–0.5	TADV+0.5
+VR	Video A/D +Vref	0.8	3.3	–0.5	VADV+0.5
–VR	Video A/D –Vref	0	2.0	–0.5	VADV+0.5
VADV	Video A/D Power	VDD–0.1	VDD+0.1		7.0
VADG	Video A/D GND	–0.1	0.1	–0.5	0.5
TADV	Thermal Head A/D Power	VDD–0.1	VDD+0.1		7.0
TADG	Thermal Head A/D GND	–0.1	0.1	–0.5	0.5
VDD	Digital Power	4.5	5.5		7.0
GND	Digital GND	0	0	0	0

Output Signal Characteristics

Output Type	Description	VOL (V max)	IOL (mA min)	VOH (V max)	IOH (mA min)	CL (pF max)
1XC	CMOS Output	0.4	1.6	VDD–1.5	1.6	50
1XP, 2XP	High Capacitance Driver	0.4	1.6	VDD–1.5	1.6	200
2XC	CMOS Output	0.4	3.5	VDD–1.5	3.5	50
2XT	TTL Output	0.4	4	2.4	4	50
2XS	CMOS Output	0.4	3.5	VDD–1.5	3.5	50
				1.5	15	50
2XL	LED Driver	0.7	10	VDD–1.5	3.5	100
3XC	CMOS Output	0.4	6	VDD–1.5	6	50
3XP	High Capacitance Driver	0.4	6	VDD–1.5	6	700
3XT	TTL Output	0.4	6	2.4	6	50
5XC	CMOS Output	0.4	12	VDD–1.0	12	50



68-Pin PLCC



64-Pin QUIP

Figure 4. 9600 bps MONOFAX Modem Pin Assignments

Table 5. 9600 bps MONOFAX Modem Pin Assignments

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Name	I/O Type
3	1	RS1	IA
4	2	RS0	IA
5	–	NC	
6	3	NC	
8	–	EN85I	R
9	4	EN85	R
10	5	PORI	ID
11	6	XTLI	R
12	7	XTLO	R
13	8	XCLK	OD
14	9	YCLK	OD
15	10	+5VD	PWR
16	11	DCLKI	R
17	12	SYNCIN2	R
68	13	DGND1	GND
18	14	CTS	OA
19	15	TXD	IA
20	16	DCLK	OA
21	17	EYESYNC	OA
22	18	EYECLK	OA
23	19	EYEX	OA
24	20	ADIN	R
25	21	DAOUT	R
52	22	AGND1	GND
53	23	AGCIN	R
30	24	AGND2	GND
31	25	–5VA	PWR
32	26	AUXI	AC
33	27	FOUT	R
34	28	TXOUT	AA
35	-	AES	R
36	29	AEE	R
37	-	NC	
38	30	ECLKIN1	R
39	31	+5VA	PWR
40	32	CABLE1	IB
41	33	CABLE2	IB
42	34	RCVI	R
43	35	FIN	R
44	36	AOUT	R
45	37	RXIN	AB
46	38	ECLKIN2	R
47	39	ADOUT	R
48	40	DAIN	R
49	41	SYNCIN1	R
50	42	RCI	R
51	43	PORO	OE
26	44	EYEY	OA
27	45	RXD	OA
28	46	RLSD	OA
29	47	RCVO	R
7	48	RTS	IA
54	49	DGND2	GND
55	50	D7	IA/OB
56	51	D6	IA/OB
57	52	D5	IA/OB
58	53	D4	IA/OB
59	54	D3	IA/OB
60	55	D2	IA/OB
61	56	D1	IA/OB
62	57	D0	IA/OB
63	58	IRQ	OC
64	59	WRITE-R/W	IA
65	60	CS	IA
66	61	READ-φ2	IA
67	62	RS4	IA
1	63	RS3	IA
2	64	RS2	IA

Notes: 1. NC = No connection, leave pin disconnected (open).
2. R = Required overhead connection; do not connect to host equipment.

Table 6. Modem Hardware Interface Signals

Name	Type	Description	Comments
Overhead Signals			
XTLI	R	Crystal/Clock Input	Connect to 24.00014 MHz Crystal (26.39998 MHz for R96VFX)
XTLO	R	Crystal Output	Connect to Crystal
PORO	OE	Power-On-Reset Output	Not used - NC (leave open)
PORI	ID	Power-On-Reset Input	Connect to IFC /MRES
+5VD	PWR	Digital +5V Supply	Connect to +5V
+5VA	PWR	Analog +5V Supply	Connect to +5V through 3 Ω
–5VA	PWR	Analog –5V Supply	Connect to –5V
DGND1, DGND2	DGND	Digital Ground	Connect to Ground
AGND1, AGND2	AGND	Analog Ground	Connect to Ground
System Bus Interface			
D0-D7	IA/OB	Data Bus Line 0-7	Connect to System Bus D0-D7
RS0-RS4	IA	Register Select 0-4	Connect to System Bus A0-A4
CS	IA	Chip Select	Connect to IFC /MCS
READ	IA	Read Enable	Connect to System Bus /RD
WRITE	IA	Write Enable	Connect to System Bus /WR
IRQ	OC	Interrupt Request	Connect to IFC /MIRQ
Auxiliary Signals			
EN85	R	Enable 85 Bus	Connect to GND though 10K Ω
CABLE1	IB	Cable Select 1	Connect to +5V or GND
CABLE2	IB	Cable Select 2	Connect to +5V or GND
XCLK	OD	X Clock Output (XTLI/2)	Connect to IFC SYSCLK
YCLK	OD	Y Clock Output (XTLI/4)	Not used - NC (leave open)
Analog Signals			
TXOUT	AA	Transmit Analog Output	Connect to Smoothing Filter Input
RXIN	AB	Receive Analog Input	Connect to Anti-aliasing Filter Output
Modem Interconnect (MI)			
EN85I	R	Modem Interconnect	Connect to EN85
DCLKI	R	Modem Interconnect	Connect to DCLK
DCLK	R	Modem Interconnect	Connect to DCLKI
ECLKIN1	R	Modem Interconnect	Connect to EYECLK
ECLKIN2	R	Modem Interconnect	Connect to EYECLK
SYNCIN1	R	Modem Interconnect	Connect to EYESYNC
SYNCIN2	R	Modem Interconnect	Connect to EYESYNC
RCVI	R	Modem Interconnect	Connect to RCVO
RCVO	R	Modem Interconnect	Connect to RCVI
ADIN	R	Modem Interconnect	Connect to ADOUT
ADOUT	R	Modem Interconnect	Connect to ADIN
DAIN	R	Modem Interconnect	Connect to DAOUT
DAOUT	R	Modem Interconnect	Connect to DAIN
FIN	R	Modem Interconnect	Connect to FOUT
FOUT	R	Modem Interconnect	Connect to FIN
AEE	R	Modem Interconnect	Connect to AGND
AES	R	Modem Interconnect	Connect to AGND
AGCIN	R	Modem Interconnect	Connect as shown in Figure 7
AOUT	R	Modem Interconnect	Connect as shown in Figure 7
RCI	R	Modem Interconnect	Connect as shown in Figure 7
TXD	IA	Transmit Data	Connect to pullup
RTS	IA	Request to Send	Connect to +5V through 10K Ω
RXD	OA	Received Data	Not used - NC (leave open)
CTS	OA	Clear to Send	Not used - NC (leave open)
RLSD	OA	Received Line Signal Detected	Not used - NC (leave open)
AUXI	AC	Auxiliary Analog Input	Not used - Connect to GND
EYEX	OA	Serial Eye Pattern X Output	Not used - NC (leave open)
EYEY	OA	Serial Eye Pattern Y Output	Not used - NC (leave open)
EYECLK	OA	Serial Eye Pattern Clock	Connect to ECLKIN1 and ECLKIN2
EYESYNC	OA	Serial Eye Pattern Strobe	Connect to SYNCIN1 and SYNCIN2

FIRMWARE DESCRIPTION

CORE PRIMITIVES AND MACROS

The R96FE firmware includes proprietary core primitives and macros which occupy approximately 8 kbytes of ROM at the top of the FAXENGINE processor address space. These core primitives and macros provide the following functions:

1. Low level subroutines (primitives) for accessing the FAXENGINE hardware.
2. High level subroutines (macros) which are common to fax machine implementations.
3. Real-time multitasking executive for scheduling high priority (interrupt-driven) tasks and servicing low priority (background) tasks.

The firmware organization is illustrated in Figure 5. The core subroutines are organized with a modular layered structure which allows for the replacement of any of the core subroutines by OEM-written custom subroutines.

Low Level Subroutines (Primitives)

The core primitives support the following:

1. Modem control
2. T.30 protocol
3. T.4 compressor/decompressor control
4. Scanner control
5. Printer control
6. Operator panel control
   a. Keypad
   b. LED
   c. LCD
   d. Beeper
7. General purpose I/O
   a. Document/paper sense/control
   b. DAA control
8. Miscellaneous functions
   a. Memory fill, copy, checksum, etc.
   b. Text-to-bitmap conversion

These routines are implemented as callable subroutines, interrupt-driven state machines, background task state machines, or a combination thereof. Detailed descriptions of these functions may be found in the R96FE FAXENGINE Evaluation System Developer's Guide.

High Level Subroutines (Macros)

The core macros are high level functions common to the operation of standard fax machines (i.e., CCITT compatible operations for transmit and receive). These macro functions simplify the implementation of common operations. Provisions for customization are provided in the R96FE FAXENGINE Evaluation System Developer's Guide. The following functions are implemented:

1. Scan document handling (e.g., pull-in and eject)
2. Printer paper handling (e.g., eject and cut)
3. Copy page
4. Send page
5. Receive page

FAXENGINE MEMORY MAP

Figure 6 shows two configurations of the FAXENGINE memory map.

One configuration supports shading correction on an 8-pixel group basis. In this configuration, 256 bytes of internal RAM are used for correction.

The other configuration supports shading correction on an individual pixel basis. In this configuration, 2048 bytes of internal RAM are used for correction. Also, a minimum of 2048 bytes of external RAM are required to support other internal IFC functions.

FAXENGINE INTERFACE CIRCUIT

Figure 7 shows the recommended interface circuits to connect the R96FE device set to the OEM electronics.

PACKAGING

Figure 8 defines the outline and dimensions of the IFC 160-pin PQFP.

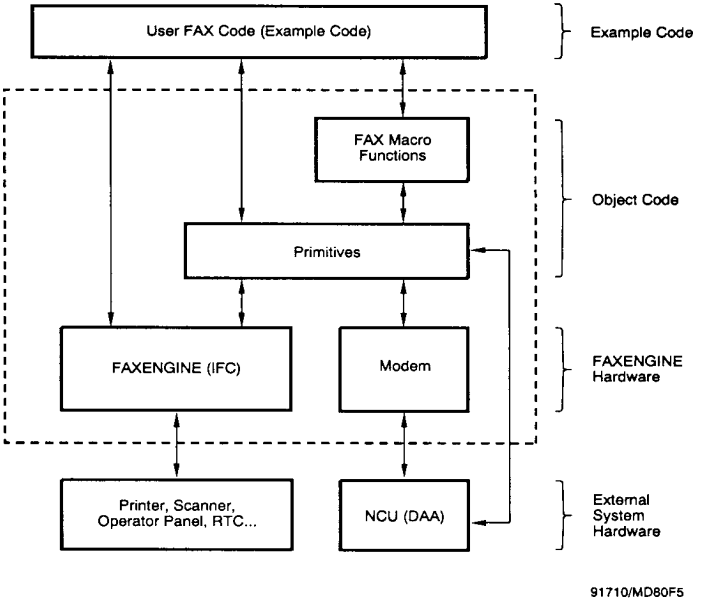
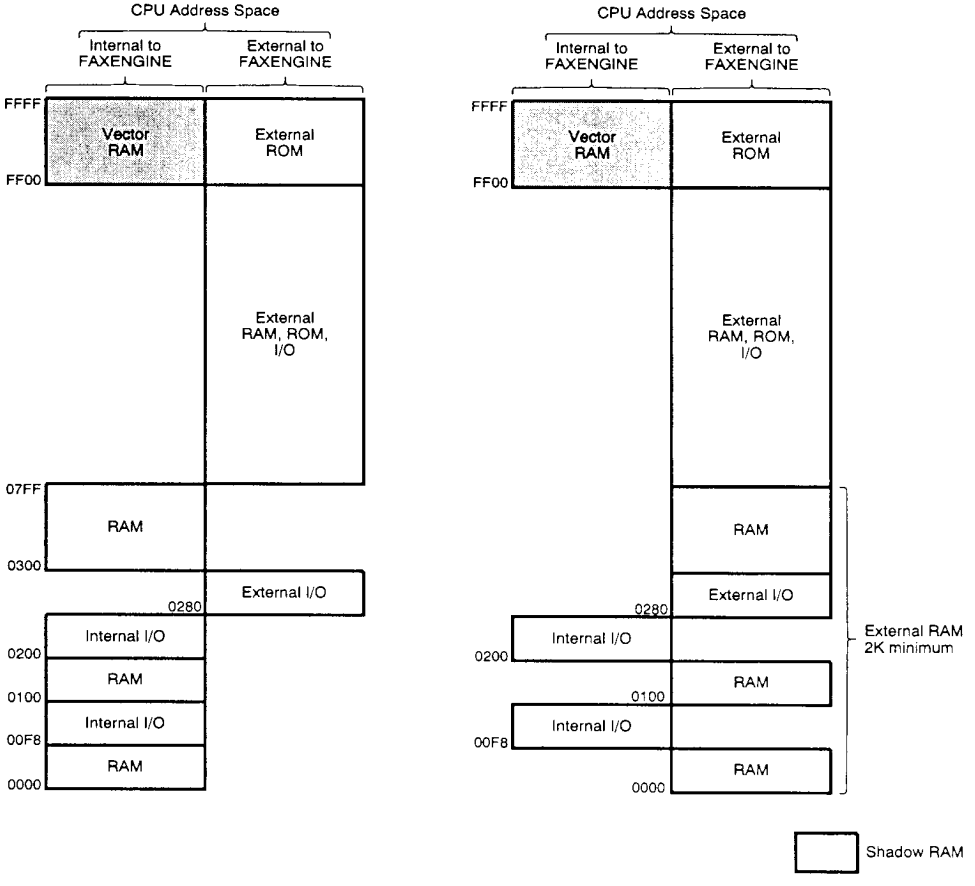


Figure 5. Software Interfaces



a. 8-Pixel Group Correction Mode

b. Individual Pixel Correction Mode

91710/MD80F6

Figure 6. R96FE Firmware Memory Map

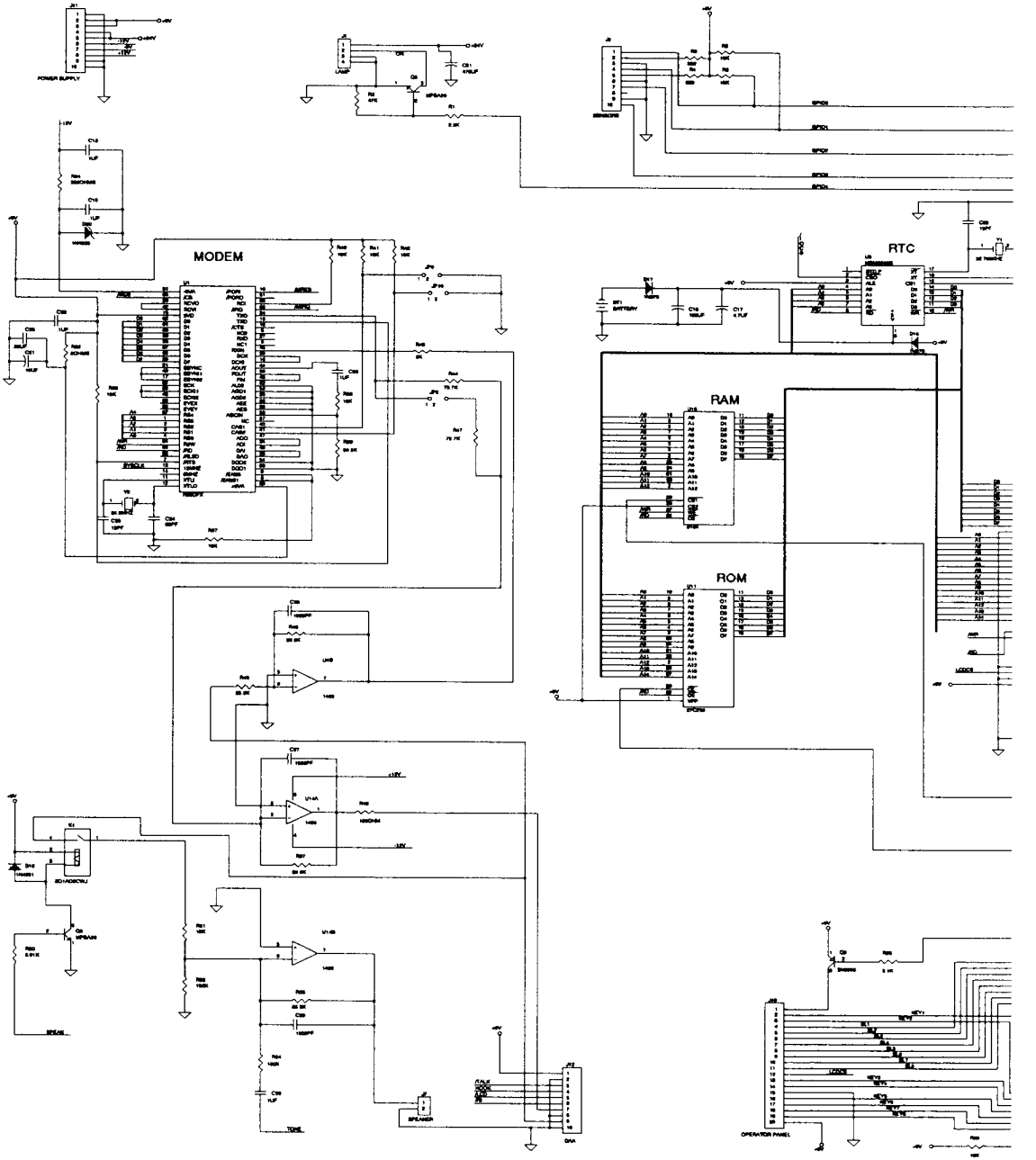


Figure 7. R96FE Interface Schematic

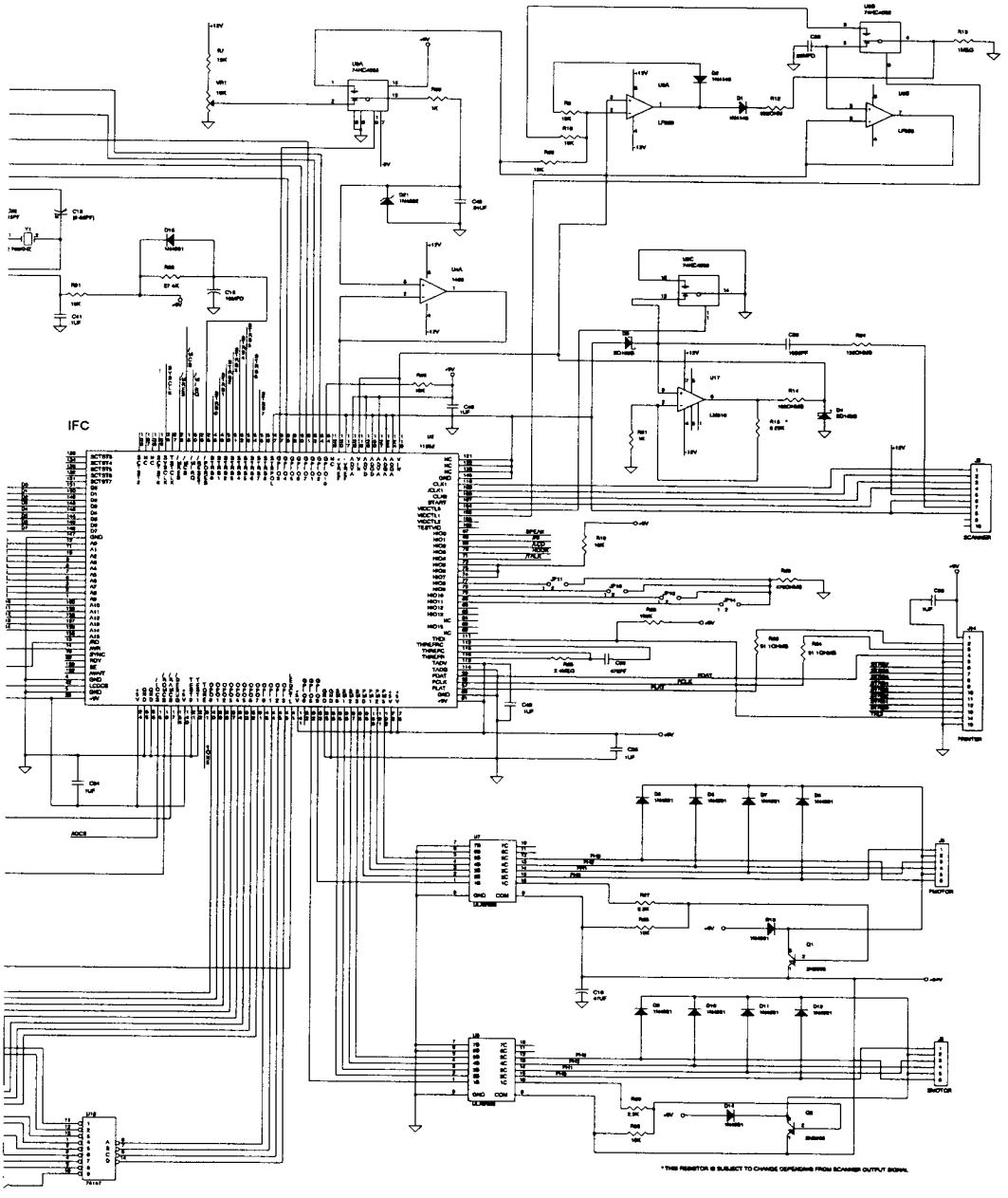
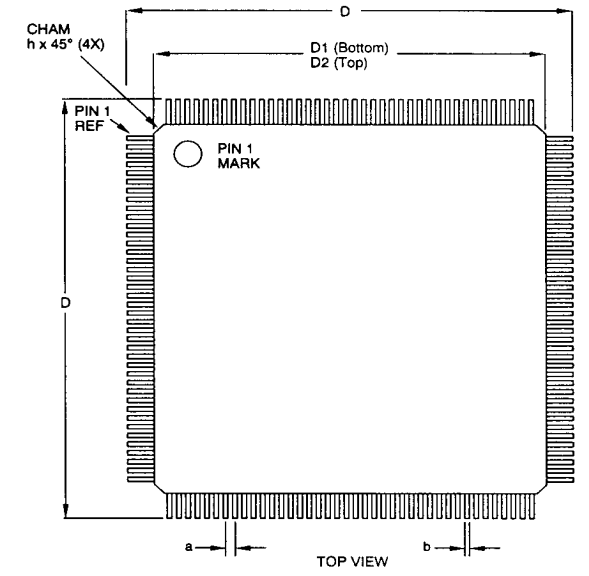
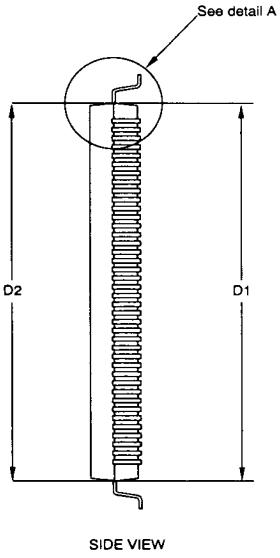
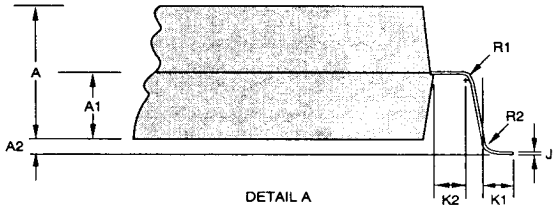


Figure 7. R96FE Interface Schematic (Cont'd)





Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	3.25	3.55	0.128	0.140
A1	1.63	1.77	0.064	0.070
A2	0.15	0.25	0.006	0.010
D	31.05	31.35	1.222	1.234
D1	27.95	28.05	1.100	1.104
D2	27.75	27.85	1.093	1.096
K1	0.70	0.90	0.028	0.035
K2	0.40 MIN		0.016 MIN	
R1	0.08	0.18	0.003	0.007
R2	0.26	0.36	0.010	0.014
a	0.60	0.70	0.024	0.028
b	0.25	0.35	0.010	0.014
h	0.6 MAX		0.024 MAX	
J	0.11	0.15	0.003	0.007
Ref: GP00-D223				



91710/MD80F8

Figure 8. 160-Pin Plastic Quad Flat Package (PQFP)

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