

February 1994

### Features

- 12A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

### Description

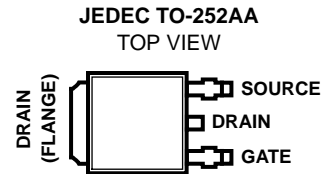
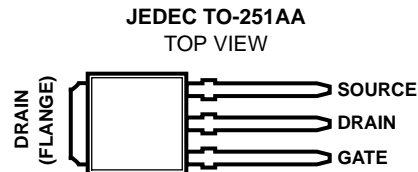
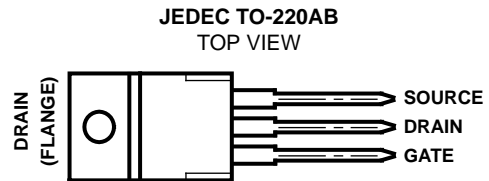
The RFD3055, RFD3055SM and RFP3055 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFD3055 is supplied in the JEDEC TO-220AB plastic package, the RFD3055SM is supplied in the JEDEC TO-252AA plastic package and the RFP3055 is supplied in the JEDEC TO-251AA plastic package. Due to space limitations the RFD3055 and RFD3055SM are branded FD3055.

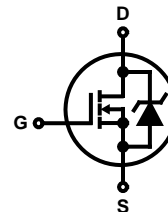
When ordering use the entire part number; eg. RFD3055SM.

Developmental type TA49082.

### Packaging



### Symbol



### Absolute Maximum Ratings (T<sub>C</sub> = +25°C), Unless Otherwise Specified

	RFD3055, RFD3055SM, RFP3055	UNITS
Drain Source Voltage . . . . .	V <sub>DSS</sub> 60	V
Drain Gate Voltage . . . . .	V <sub>DGR</sub> 60	V
Gate Source Voltage . . . . .	V <sub>GS</sub> ±20	V
Drain Current		
RMS Continuous . . . . .	I <sub>D</sub> 12	A
Pulsed Drain Current . . . . .	I <sub>DM</sub> Refer to Peak Current Curve	
Pulsed Avalanche Rating . . . . .	E <sub>AS</sub> Refer to UIS Curve	
Maximum Avalanche Current . . . . .	I <sub>AM</sub> 30	A
Power Dissipation		
T <sub>C</sub> = +25°C . . . . .	P <sub>D</sub> 53	W
Derate above +25°C . . . . .	P <sub>T</sub> 0.357	W/°C
Operating and Storage Temperature . . . . .	T <sub>STG</sub> , T <sub>J</sub> -55 to +175	°C

## Specifications RFD3055, RFD3055SM, RFP3055

### Electrical Specifications $T_C = +25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D = 0.25\text{mA}$ , $V_{GS} = 0\text{V}$	60	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 0.25\text{mA}$	2	-	4	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$	$T_C = +25^\circ\text{C}$	-	-	1	$\mu\text{A}$
			$T_C = +150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
On Resistance	$r_{DS(ON)}$	$I_D = 12\text{A}$ , $V_{GS} = 10\text{V}$	-	-	0.150	W	
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}$ , $I_D = 12\text{A}$ $R_L = 2.5\Omega$ , $V_{GS} = +10\text{V}$ $R_{GS} = 10\Omega$	-	-	40	ns	
Turn-On Delay Time	$t_{D(ON)}$		-	7	-	ns	
Rise Time	$t_R$		-	21	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		-	16	-	ns	
Fall Time	$t_F$		-	10	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	40	ns	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 0$ to $20\text{V}$	$V_{DD} = 48\text{V}$ , $I_D = 12\text{A}$ , $R_L = 4\Omega$	-	19	23
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0$ to $10\text{V}$	-		10	12	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $2\text{V}$	-		0.6	0.8	nC
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 12\text{A}$ , $V_{DS} = 15\text{V}$	-	-	7.5	V	
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	300	-	pF	
Output Capacitance	$C_{OSS}$		-	100	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	30	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	2.8	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251 and TO-252 Package	-	-	100	$^\circ\text{C/W}$	
		TO-220 Package	-	-	80	$^\circ\text{C/W}$	

### Source-Drain Diode Ratings and Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Forward Voltage	$V_{SD}$	$I_{SD} = 12\text{A}$	-	-	1.5	V
Reverse Recovery Time	$t_{RR}$	$I_{SD} = 12\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns

Typical Performance Curves

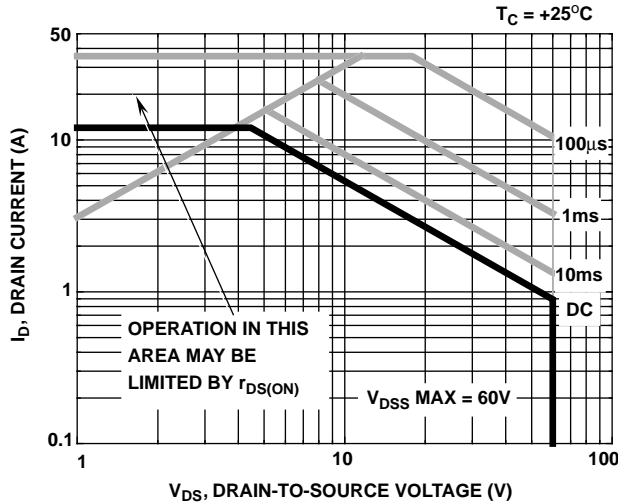


FIGURE 1. SAFE- OPERATING AREA CURVE

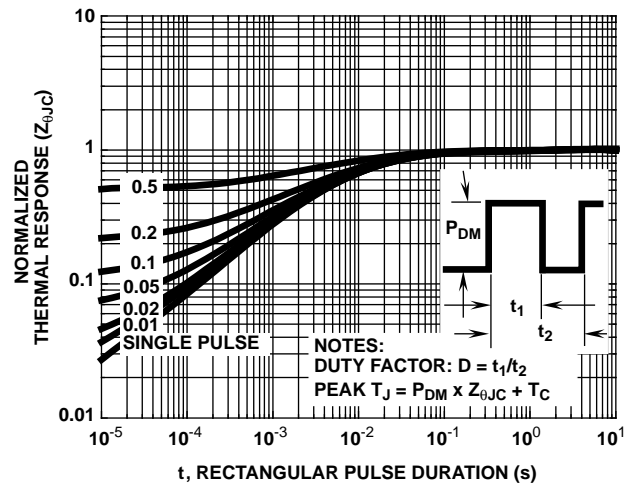


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

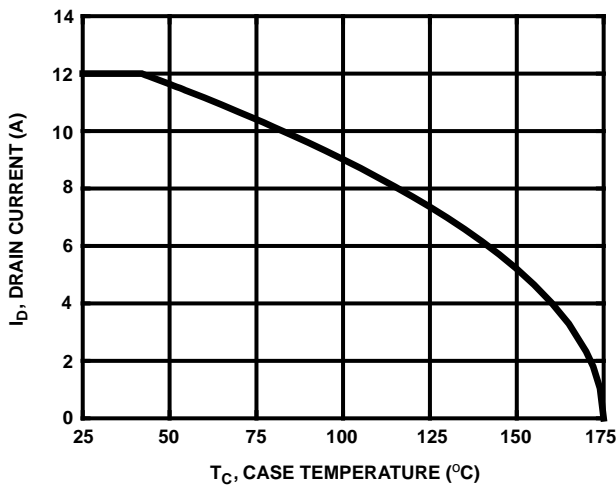


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

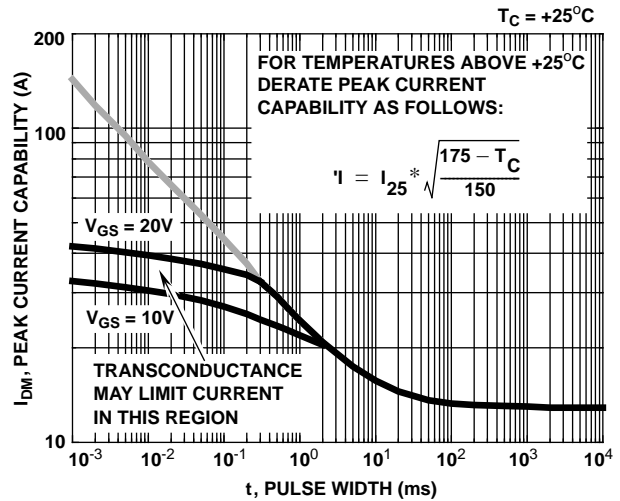


FIGURE 4. PEAK CURRENT CAPABILITY

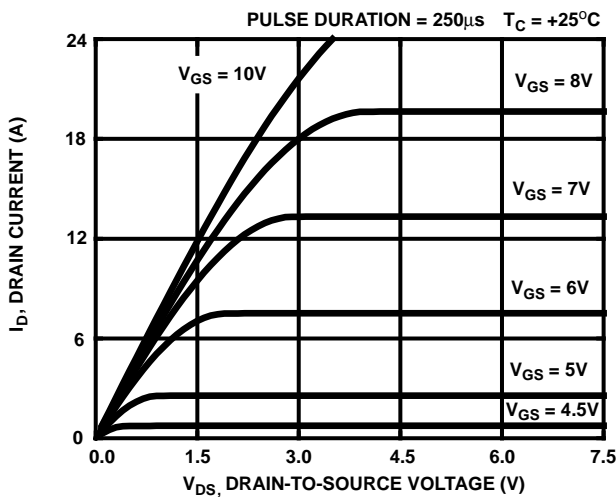


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

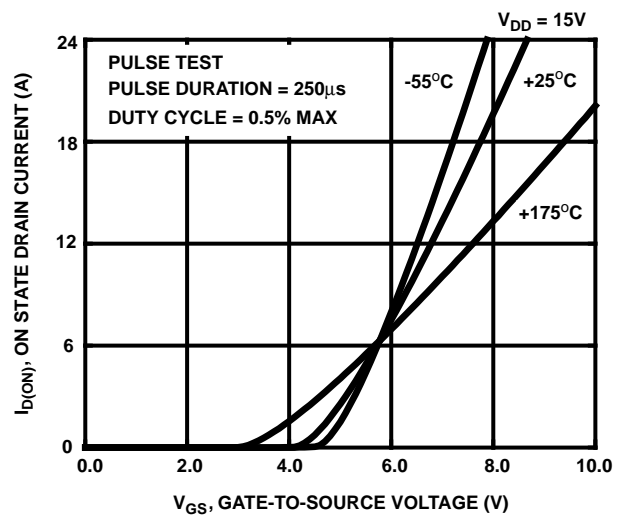


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

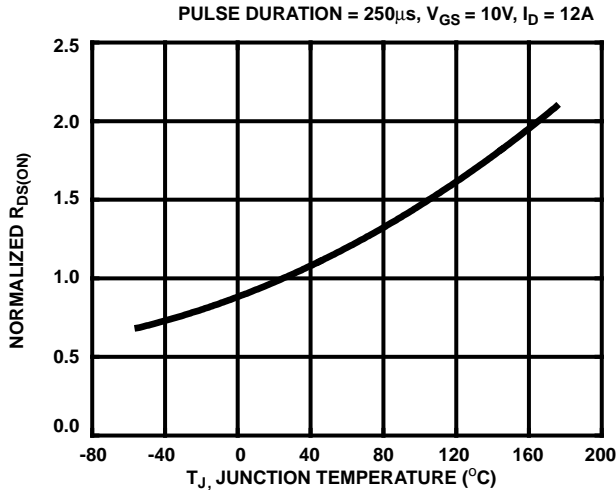


FIGURE 7. NORMALIZED  $R_{DS(ON)}$  vs JUNCTION TEMPERATURE

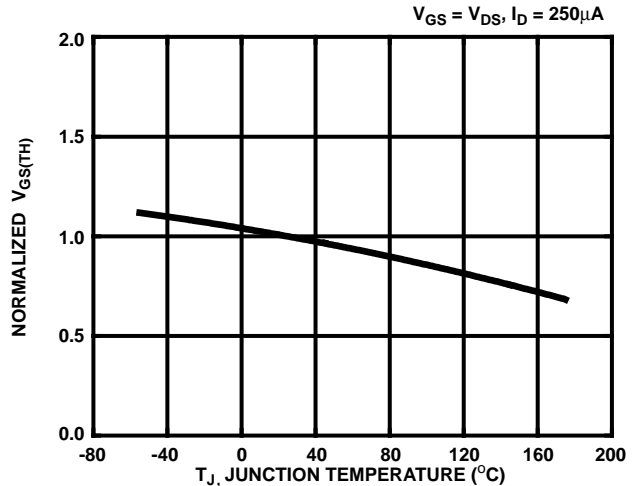


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

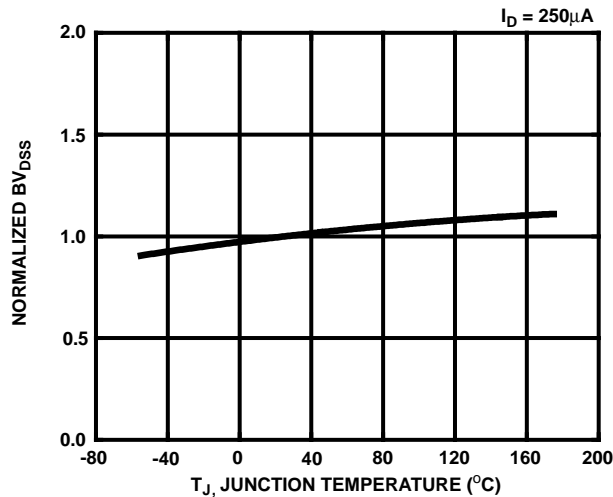


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

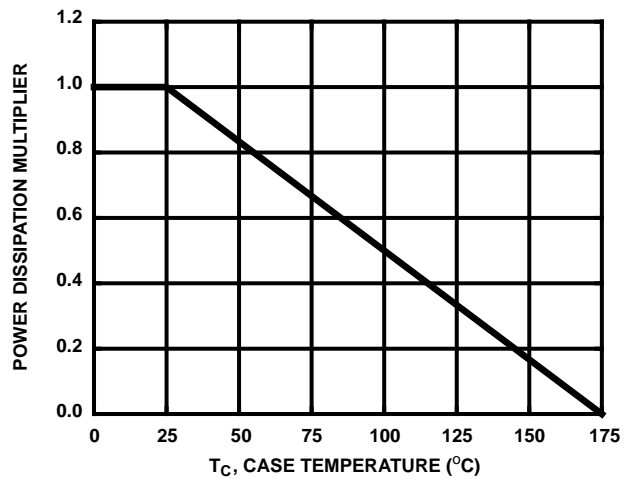


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

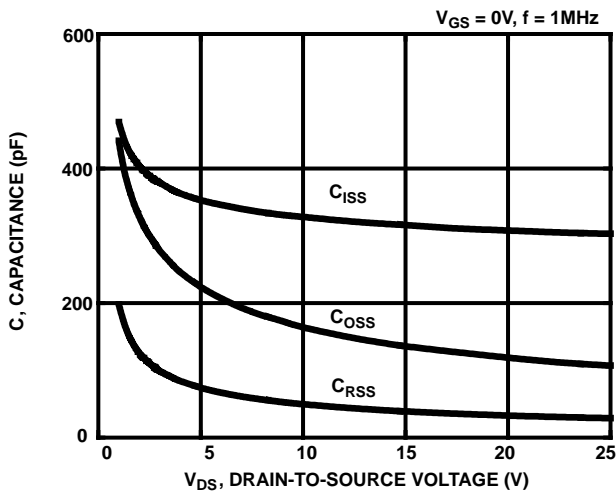


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

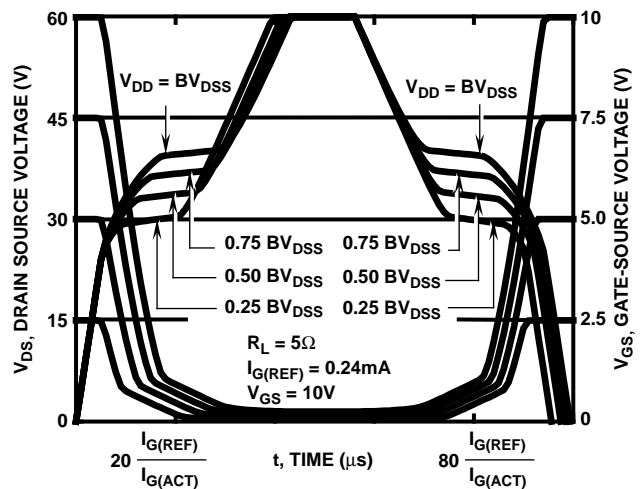


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

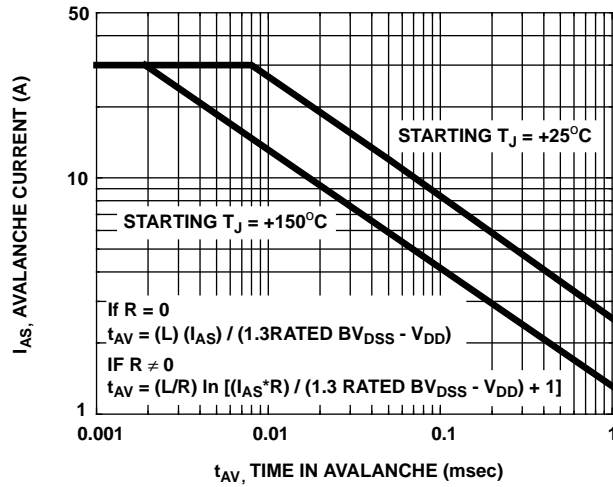


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

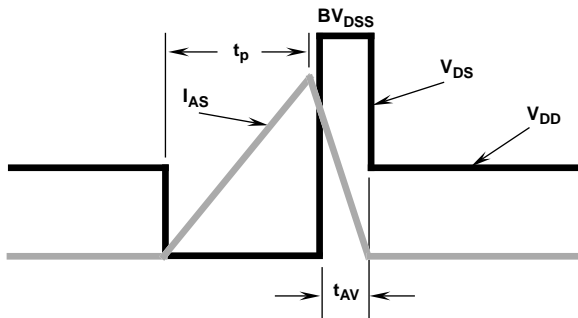


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

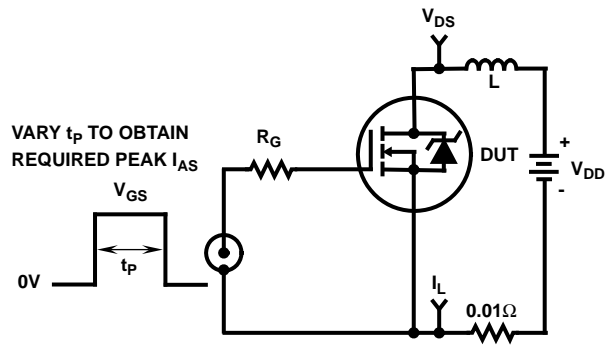


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

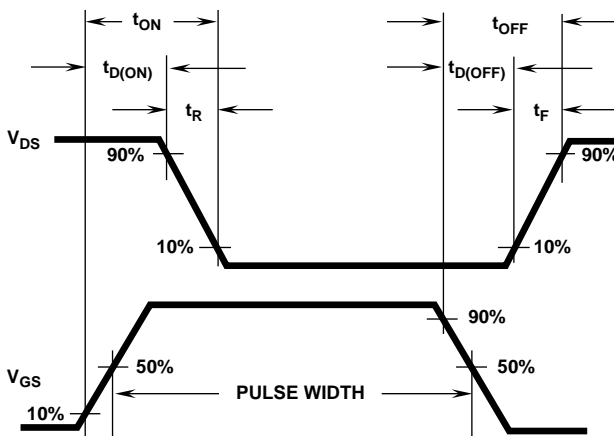


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

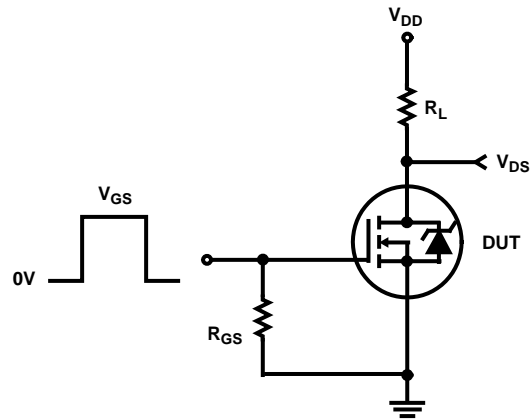


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

## RFD3055, RFD3055SM, RFP3055

### PSpice Model Listing

#### Temperature Compensated PSPICE Model for the RFD3055, RFD3055SM, RFP3055

.SUBCKT RFP3055 2 1 3; rev 10/26/93

CA 12 8 0.540e-9  
 CB 15 14 0.540e-9  
 CIN 6 8 0.300e-9

DBODY 7 5 DBDMOD  
 DBREAK 5 11 DBKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 67.9  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 4.61e-9  
 LSOURCE 3 7 4.61e-9

MOS1 16 6 8 8 MOSMOD M=0.99  
 MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1  
 RDRAIN 50 16 RDSMOD 1e-4  
 RGATE 9 20 7.23  
 RIN 6 8 1e9  
 RSCL1 5 51 RSLVCMOD 1e-6  
 RSCL2 5 50 1e3  
 RSOURCE 8 7 RDSMOD 108e-3  
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

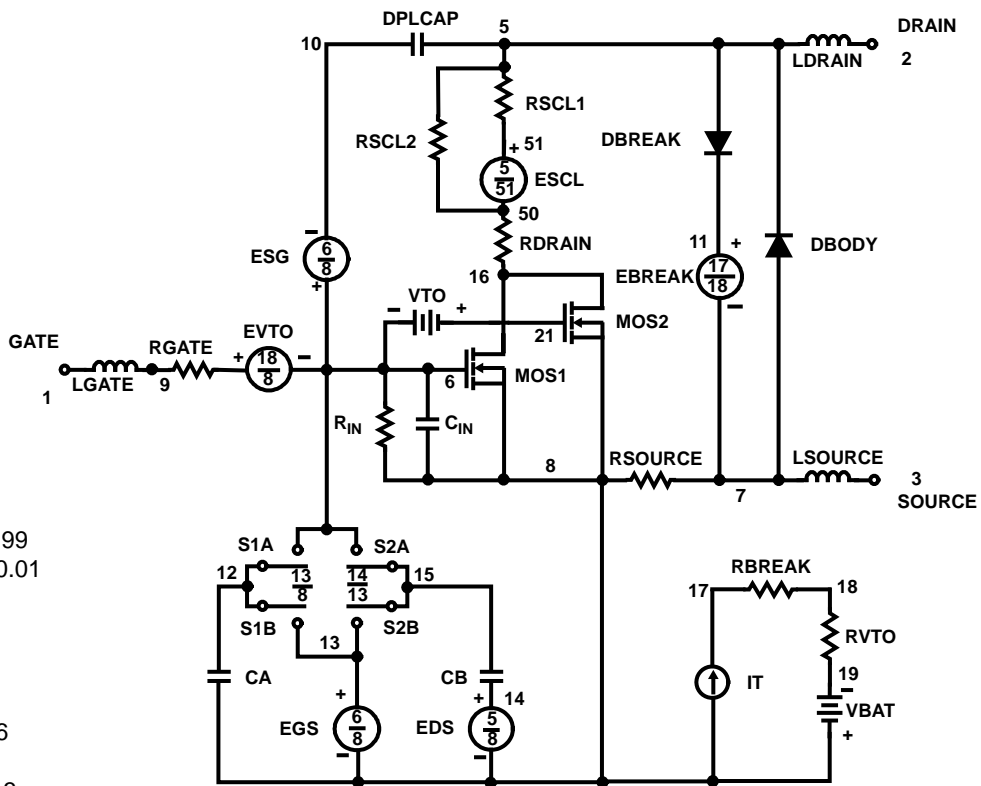
VBAT 8 19 DC 1  
 VTO 21 6 0.5

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))\*1e6/30,6.5)}

.MODEL DBDMOD D (IS=4.33e-14 RS=2.78e-2 TRS1=1.10e-3 TRS2=5.19e-6 CJO=3.94e-10 TT=7.63e-8)  
 .MODEL DBKMOD D (RS=0.676 TRS1=1.94e-3 TRS2=-1.09e-6)  
 .MODEL DPLCAPMOD D (CJO=0.238e-9 IS=1e-30 N=10)  
 .MODEL MOSMOD NMOS (VTO=4.078 KP=12 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
 .MODEL RBKMOD RES (TC1=1.06e-3 TC2=-1.92e-6)  
 .MODEL RDSMOD RES (TC1=5.03e-3 TC2=1.53e-5)  
 .MODEL RSLVCMOD RES (TC1=2.2e-3 TC2=-5e-6)  
 .MODEL RVTOMOD RES (TC1=-5.02e-3 TC2=-9.16e-6)  
 .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.5 VOFF=-3.5)  
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-6.5)  
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.50 VOFF=2.50)  
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.50 VOFF=-2.50)

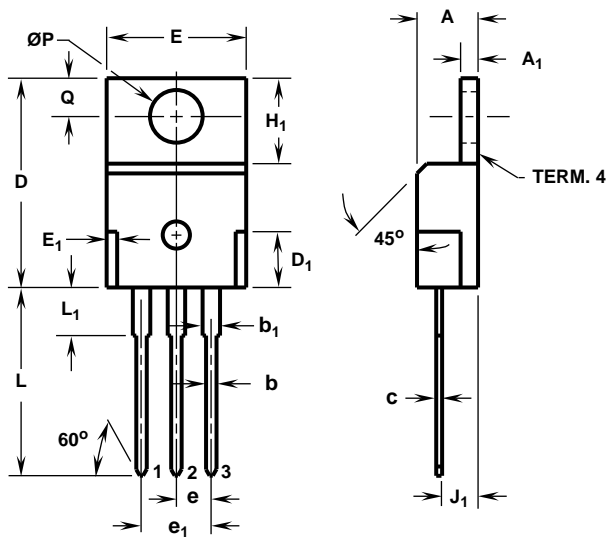
.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.



RFD3055, RFD3055SM, RFP3055

Packaging



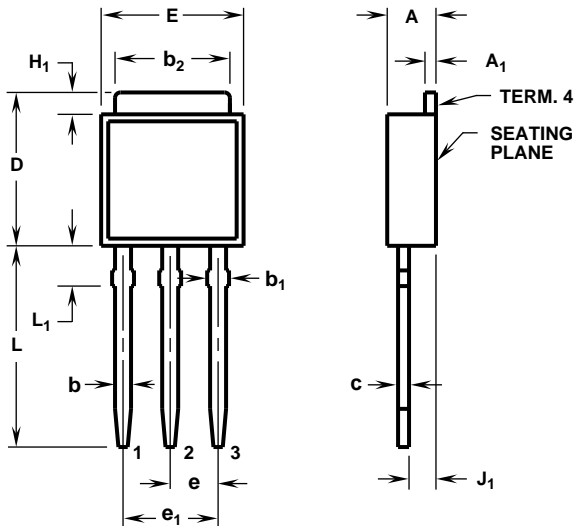
NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in  $L_1$ .
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.

TO-220AB  
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b <sub>1</sub>	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D <sub>1</sub>	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E <sub>1</sub>	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e <sub>1</sub>	0.200 BSC		5.08 BSC		5
H <sub>1</sub>	0.235	0.255	5.97	6.47	-
J <sub>1</sub>	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L <sub>1</sub>	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.



NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled.
3. Dimension (without solder).
4. Add typically 0.0006 inches (0.015mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.

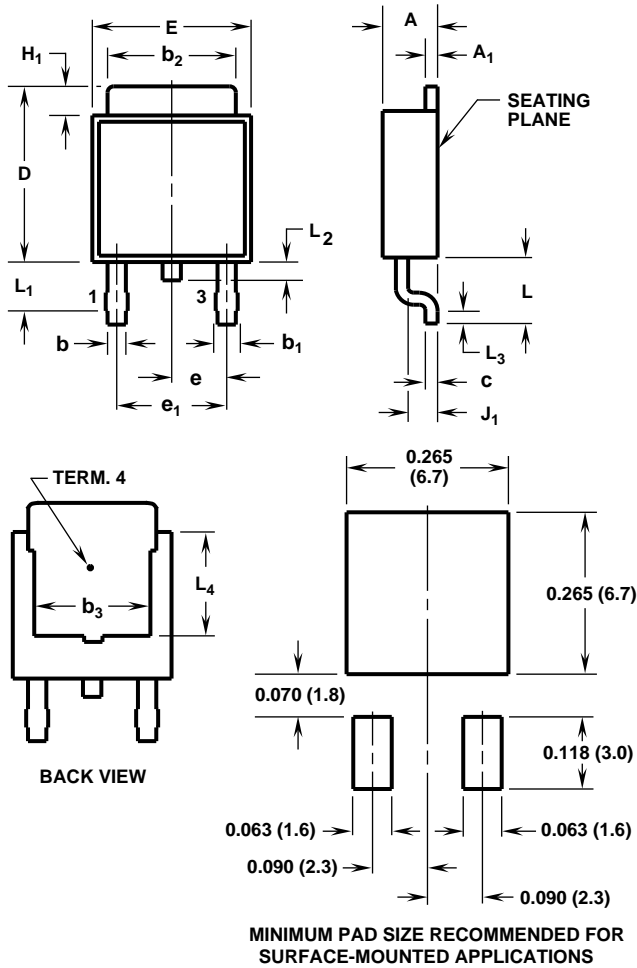
TO-251AA  
3 LEAD JEDEC TO-251AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A <sub>1</sub>	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b <sub>1</sub>	0.033	0.040	0.84	1.01	3
b <sub>2</sub>	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e <sub>1</sub>	0.180 BSC		4.57 BSC		5
H <sub>1</sub>	0.035	0.045	0.89	1.14	-
J <sub>1</sub>	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L <sub>1</sub>	0.075	0.090	1.91	2.28	2

6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Packaging (Continued)

TO-252AA  
2 LEAD JEDEC TO-252AA PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A <sub>1</sub>	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b <sub>1</sub>	0.033	0.040	0.84	1.01	4
b <sub>2</sub>	0.205	0.215	5.21	5.46	4, 5
b <sub>3</sub>	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e <sub>1</sub>	0.180 BSC		4.57 BSC		7
H <sub>1</sub>	0.035	0.045	0.89	1.14	-
J <sub>1</sub>	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L <sub>1</sub>	0.075	0.090	1.91	2.28	3
L <sub>2</sub>	0.025	0.040	0.64	1.01	-
L <sub>3</sub>	0.020	-	0.51	-	4, 6
L <sub>4</sub>	0.170	-	4.32	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L<sub>4</sub> and b<sub>3</sub> dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled.
4. Dimension (without solder).
5. Add typically 0.0006 inches (0.015mm) for solder coating.
6. L<sub>3</sub> is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 2 dated 6-93.

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