SGMOP07E
600kHz, Low Noise, High Voltage, Precision Operational Amplifier

GENERAL DESCRIPTION

The SGMOP07E is a single, low noise, low offset voltage and high voltage operational amplifier, which can operate from 3.6V to 36V single supply or from ±1.8V to ±18V dual supplies, while consuming only 0.75mA quiescent current.

The SGMOP07E is well suited in low noise systems. It exhibits a high gain-bandwidth product of 600kHz and a slew rate of 3V/μs. The output swing is rail-to-rail with heavy loads. These specifications make the operational amplifiers appropriate for various applications.

The SGMOP07E is available in a Green SOIC-8 package. It is specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Low Bias Current: ±1nA (TYP)**
- **High Open-Loop Gain: 130dB at V_S = ±15V**
- **High PSRR: 135dB**
- **Gain-Bandwidth Product: 600kHz**
- **Low Noise: 8.5nV/$\sqrt{Hz}$ at 1kHz**
- **Rail-to-Rail Output**
- **Supply Voltage Range:**
  3.6V to 36V or ±1.8V to ±18V
- **Input Common Mode Voltage Range:**
  ($-V_S$) + 1.5V to ($+V_S$) - 2V
- **Low Quiescent Current: 0.75mA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-8 Package**

APPLICATIONS

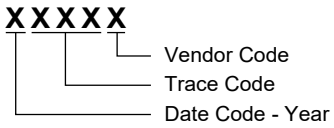
Sensors
Audio
Active Filters
A/D Converters
Communications
Test Equipment
Cellular and Cordless Phones
Laptops and PDAs
Photodiode Amplification

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMOP07E	SOIC-8	-40℃ to +125℃	SGMOP07EXS8G/TR	SGM OP07EXS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input Common Mode Voltage Range
..... $(-V_S)$ - 0.3V to $(+V_S)$ + 0.3V
Package Thermal Resistance @ T_A = +25℃
SOIC-8, θ_{JA} ..... 105℃/W
SOIC-8, θ_{JB} ..... 57℃/W
SOIC-8, θ_{JC} ..... 43.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
MM 250V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 3.6V to 36V
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

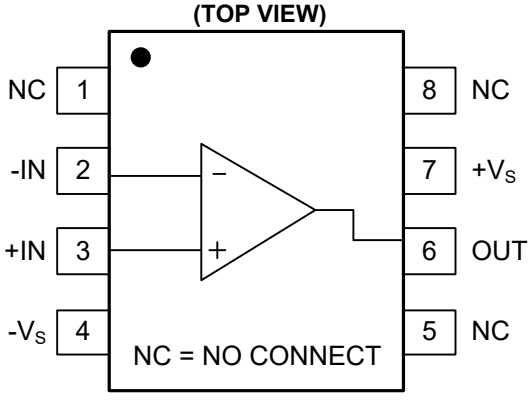
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



SOIC-8

ELECTRICAL CHARACTERISTICS

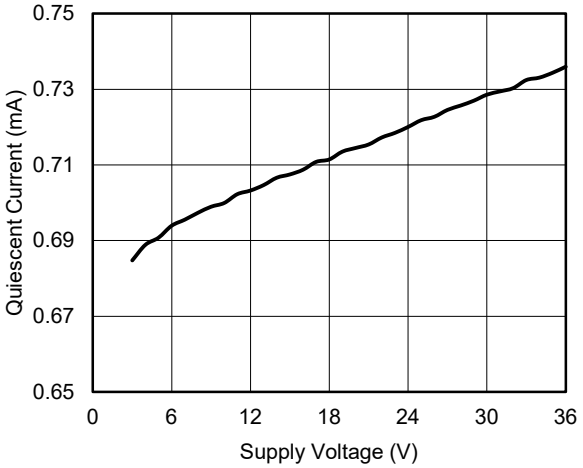
(At T_A = +25℃, V_S = ±5V to ±15V, V_{CM} = 0V, V_{OUT} = 0V and R_L = 2kΩ connected to 0V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}		+25℃		35	150	μV
			Full			220	
Input Bias Current	I_B		+25℃		±1	±12	nA
			Full			±45	
Input Offset Current	I_{OS}		+25℃		±1	±12	nA
			Full			±35	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ + 1.5		$(+V_S)$ - 2	V
Common Mode Rejection Ratio	CMRR	$(-V_S)$ + 1.5V ≤ V_{CM} ≤ $(+V_S)$ - 2V	+25℃	120	140		dB
			Full	115			
Open-Loop Voltage Gain	A_{OL}	V_S = ±5V, V_{OUT} = ±2.5V, R_L = 10kΩ	+25℃	115	135		dB
			Full	112			
		V_S = ±15V, V_{OUT} = ±10V, R_L = 10kΩ	+25℃	120	135		
			Full	117			
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 2kΩ	+25℃	110	124		
			Full	106			
		V_S = ±15V, V_{OUT} = ±10V, R_L = 2kΩ	+25℃	120	130		
			Full	112			
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		0.3		μV/℃
Output Characteristics							
Output Voltage Swing from Rail	V_{OUT}	V_S = ±15V, R_L = 10kΩ	+25℃		90	120	mV
			Full			165	
		V_S = ±15V, R_L = 2kΩ	+25℃		450	600	
			Full			820	
Output Short-Circuit Current	I_{SC}	V_S = ±15V	+25℃	±21	±34		mA
Power Supply							
Operating Voltage Range	V_S		Full	3.6		36	V
Quiescent Current	I_Q	I_{OUT} = 0mA	+25℃		0.75	0.9	mA
			Full			1	
Power Supply Rejection Ratio	PSRR	V_S = 3V to 38V	+25℃	123	135		dB
			Full	120			
Dynamic Performance							
Gain-Bandwidth Product	GBP	V_{OUT} = 100mV_{P-P}, C_L = 10pF	+25℃		600		kHz
Slew Rate	SR		+25℃		3		V/μs
Settling Time to 0.1%	t_S	V_{IN} = 1V Step, G = +1	+25℃		3.5		μs
Overload Recovery Time		V_{IN} × G = V_S	+25℃		1.5		μs
Phase Margin	φ_O	V_{OUT} = 100mV_{P-P}, C_L = 10pF	+25℃		60		°
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 1V_{RMS}, G = +1, f = 1kHz	+25℃		0.0008		%
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		300		nV_{P-P}
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		8.5		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1kHz	+25℃		1.5		$pA/\sqrt{Hz}$

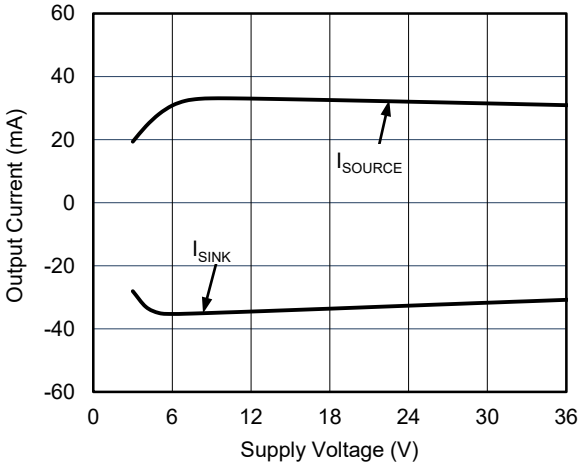
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

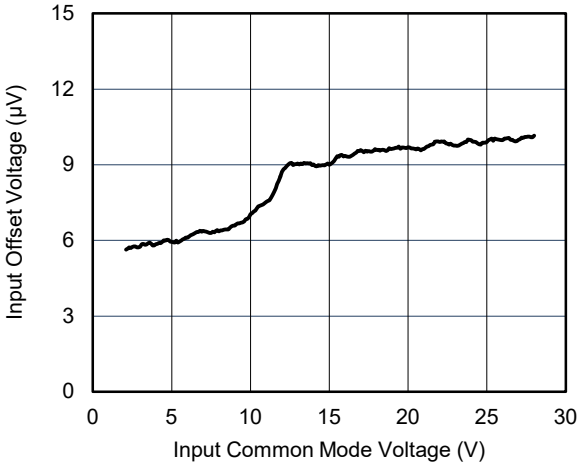
Quiescent Current vs. Supply Voltage



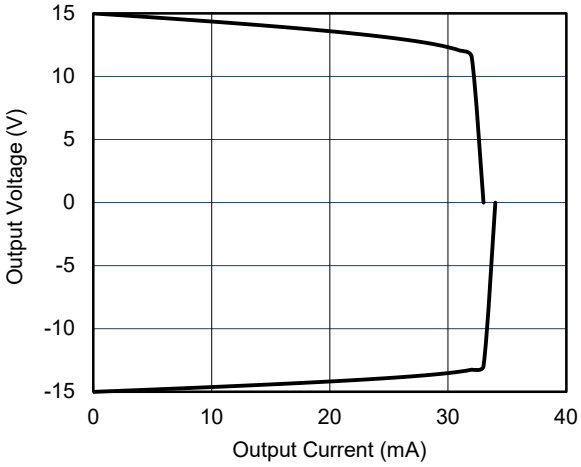
Output Current vs. Supply Voltage



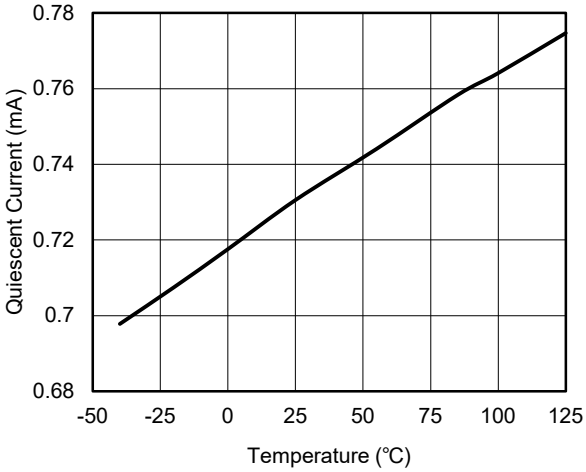
Input Offset Voltage vs. Input Common Mode Voltage



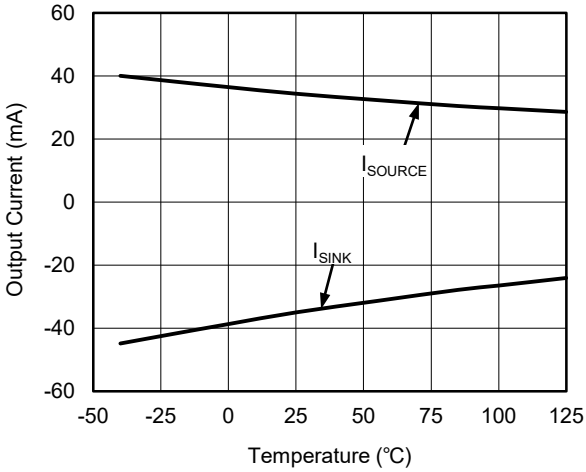
Output Voltage vs. Output Current



Quiescent Current vs. Temperature



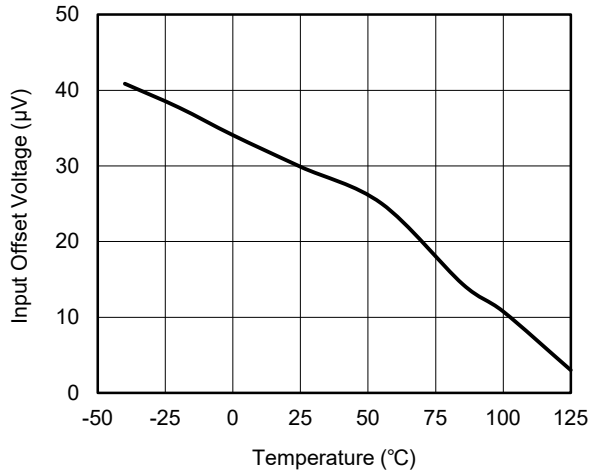
Output Current vs. Temperature



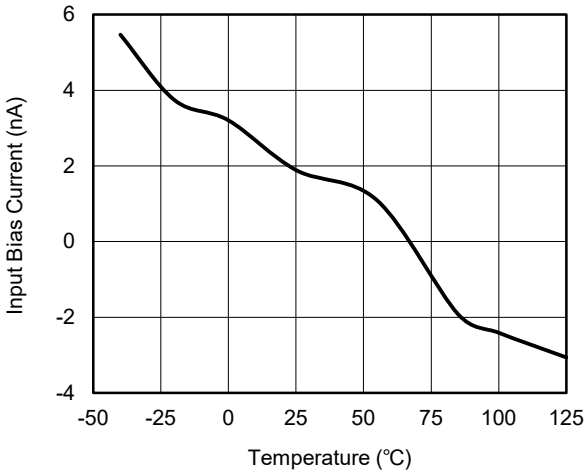
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

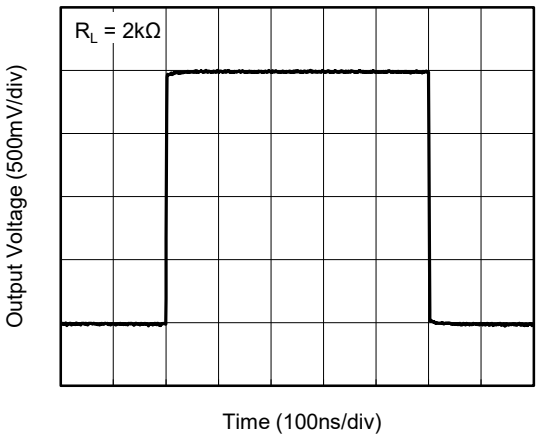
Input Offset Voltage vs. Temperature



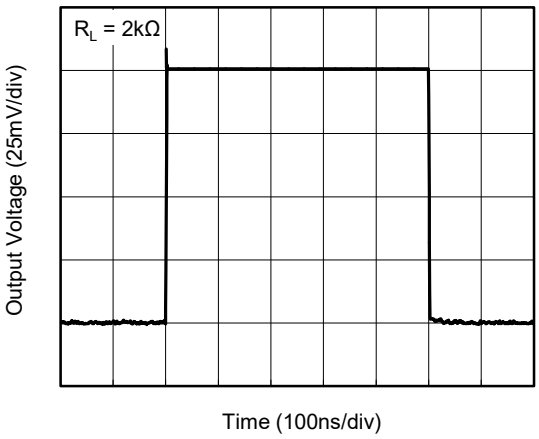
Input Bias Current vs. Temperature



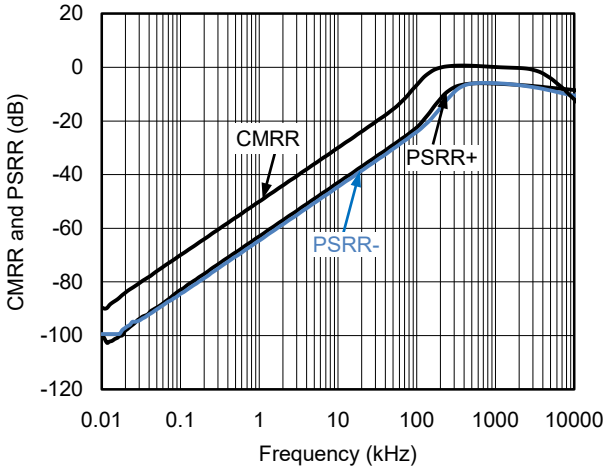
Large-Signal Step Response



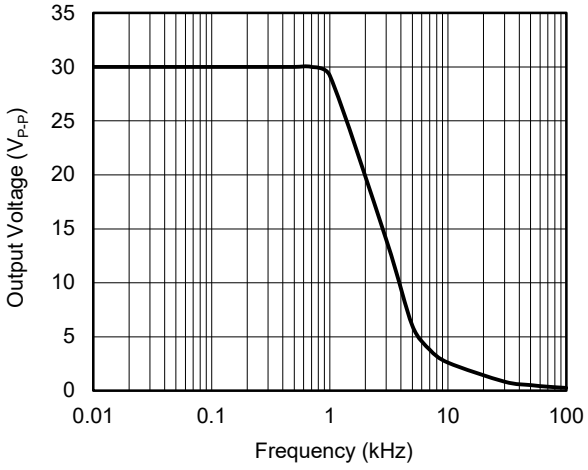
Small-Signal Step Response



CMRR and PSRR vs. Frequency



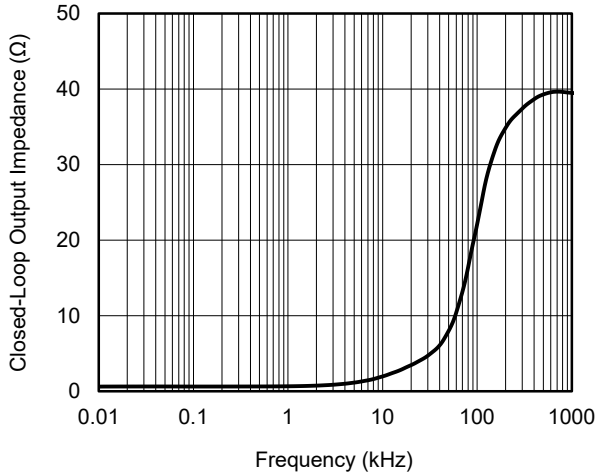
Maximum Output Voltage vs. Frequency



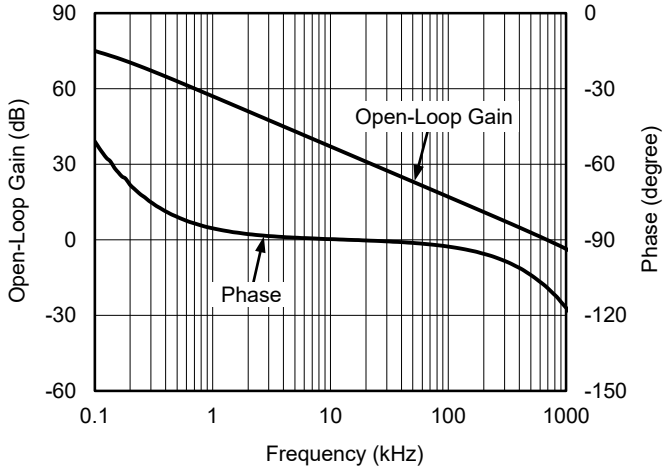
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

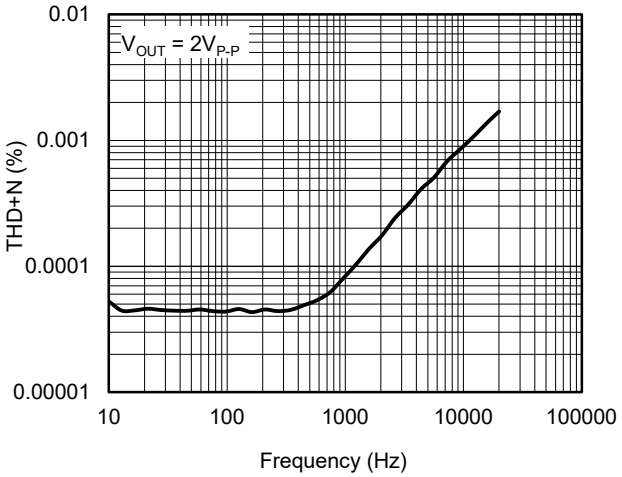
Closed-Loop Output Impedance vs. Frequency



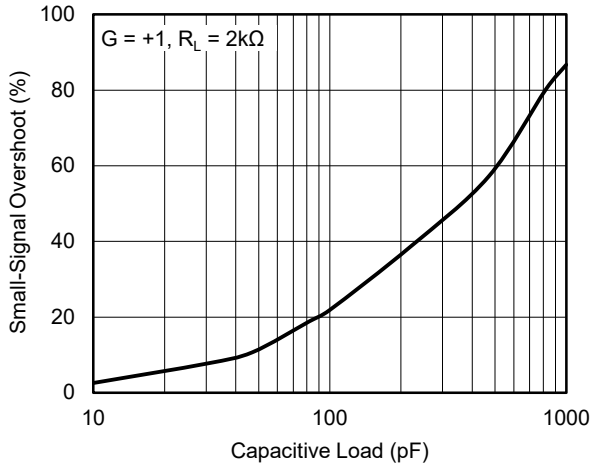
Open-Loop Gain and Phase vs. Frequency



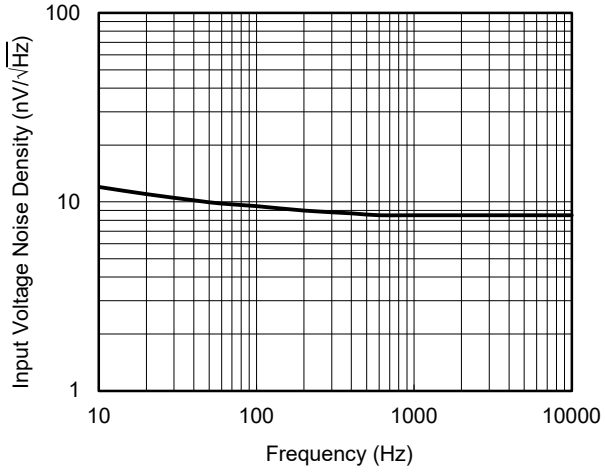
Total Harmonic Distortion + Noise vs. Frequency



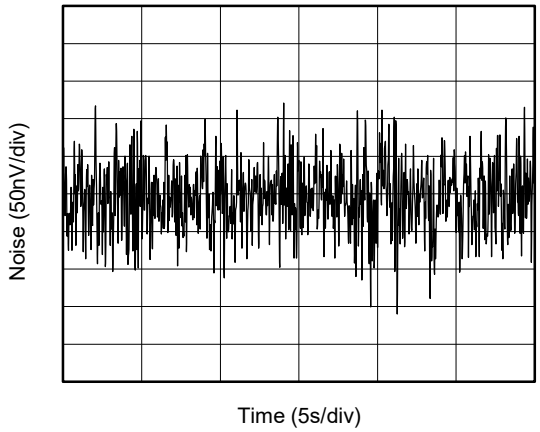
Small-Signal Overshoot vs. Capacitive Load



Input Voltage Noise Density vs. Frequency



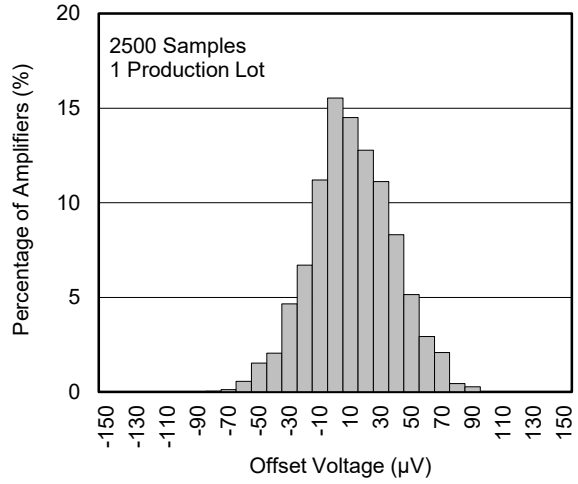
0.1Hz to 10Hz Input Voltage Noise



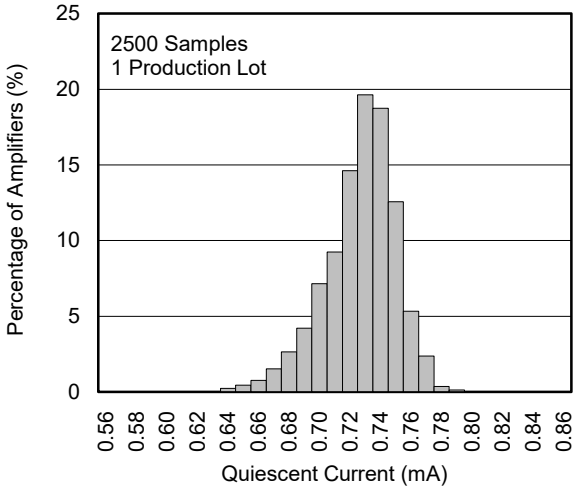
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

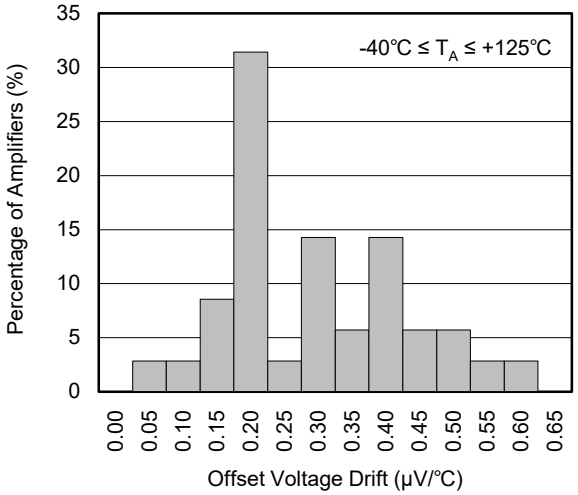
Offset Voltage Production Distribution



Quiescent Current Production Distribution



Offset Voltage Drift Distribution



APPLICATION INFORMATION

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifier through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 1. The ceramic capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

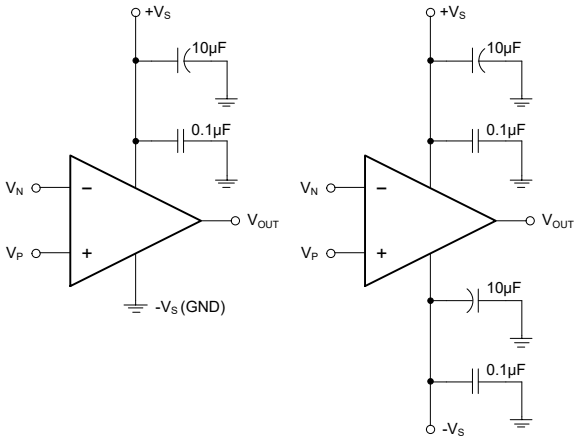


Figure 1. Amplifier Power Supply Bypassing

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

Typical Application Circuits

Difference Amplifier

The circuit in Figure 2 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

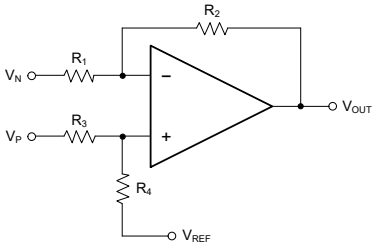


Figure 2. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 3 is a design example of high input impedance difference amplifier, the added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 2.

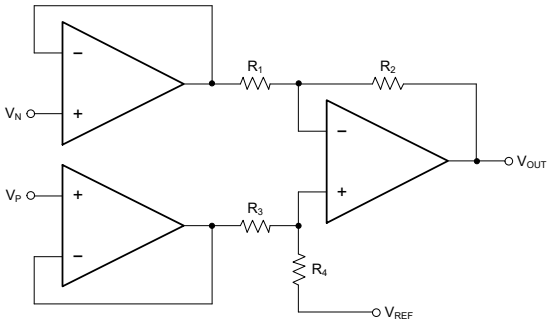


Figure 3. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 4 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/2\pi R_2 C$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

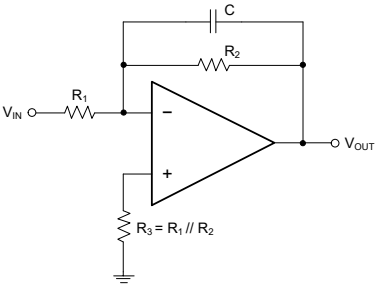


Figure 4. Active Low-Pass Filter

REVISION HISTORY

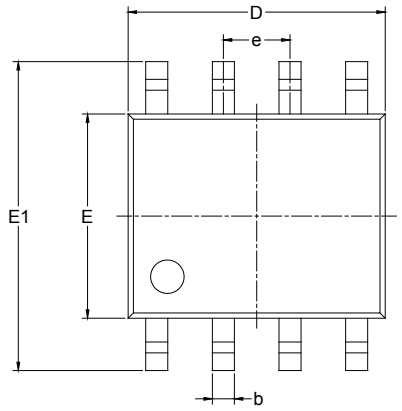
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

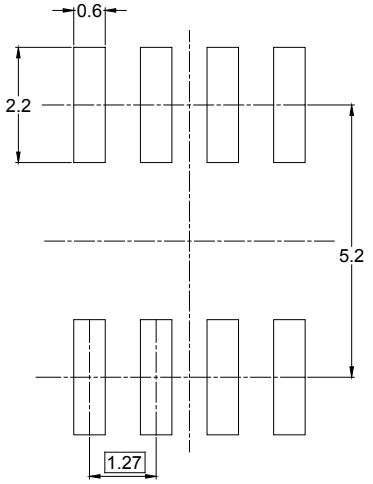
NOVEMBER 2020 – REV.A to REV.A.1	Page
Updated Marking Information section	2
Updated Absolute Maximum Ratings section	2

Changes from Original (DECEMBER 2017) to REV.A	Page
Changed from product preview to production data	All

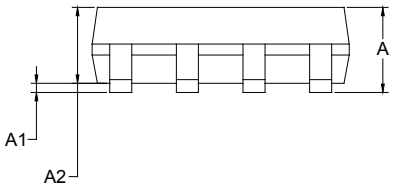
PACKAGE OUTLINE DIMENSIONS

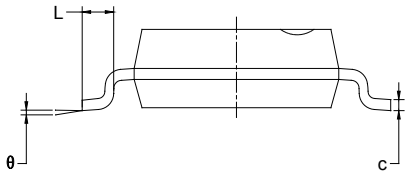
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

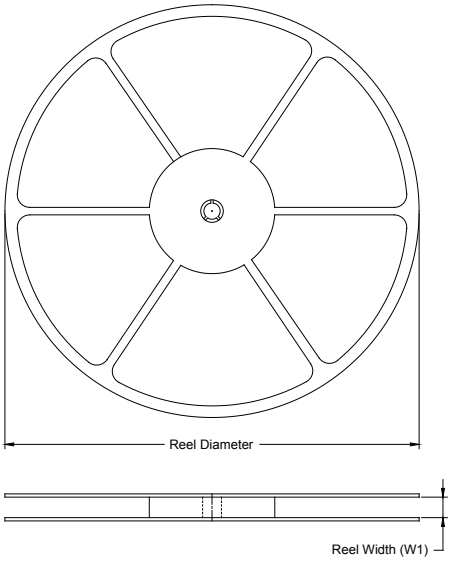




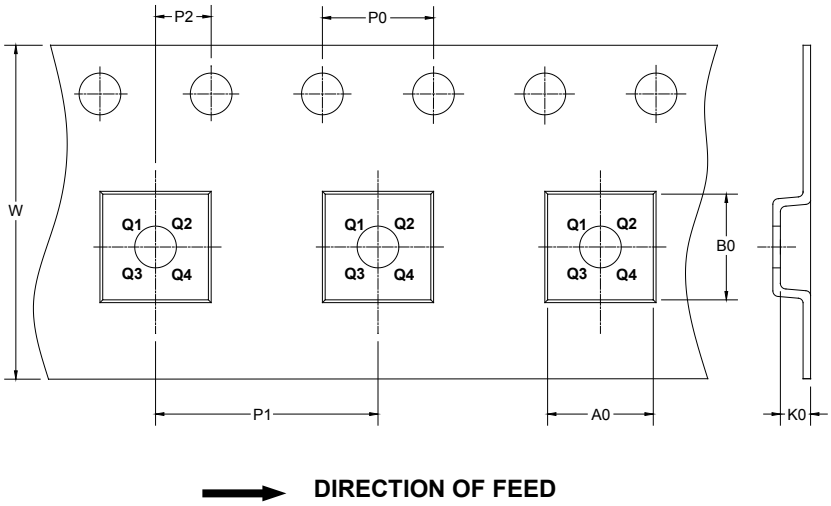
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

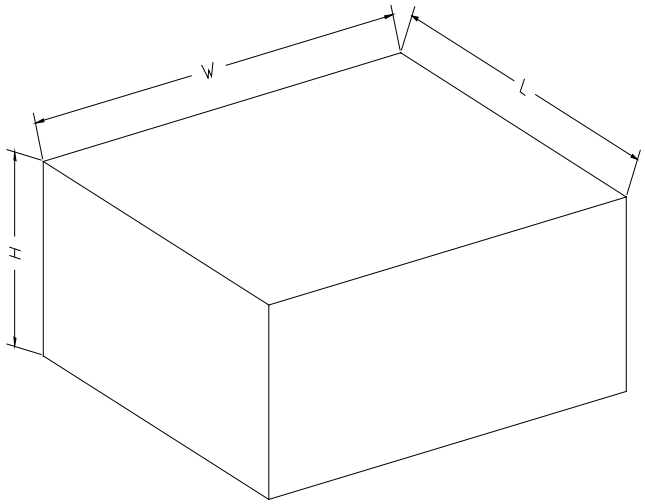
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002