



Dual N-Channel 60-V (D-S), 175°C MOSFET

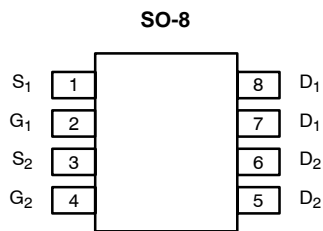
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.055 @ $V_{GS} = 10$ V	4.5
	0.075 @ $V_{GS} = 4.5$ V	3.9

FEATURES

- TrenchFET® Power MOSFET
- 175°C Maximum Junction Temperature
- 100% R_g Tested

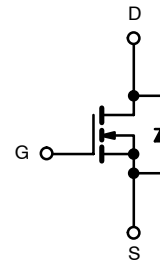


Pb-free
Available



Top View

Ordering Information: Si4946EY
Si4946EY-T1 (with Tape and Reel)
Si4946EY—E3 (Lead (Pb)-Free)
Si4946EY-T1—E3 (Lead (Pb)-Free with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	4.5
		$T_A = 70^\circ\text{C}$	3.8
Pulsed Drain Current	I_{DM}	30	A
Continuous Source Current (Diode Conduction) ^a	I_S	2	
Single Avalanche Current	$L = 0.1$ mH	I_{AS}	12
Single Avalanche Energy			E_{AS}
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.4
		$T_A = 70^\circ\text{C}$	1.7
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			2	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.5 A		0.045	0.055	Ω
		V _{GS} = 4.5 V, I _D = 3.9 A		0.055	0.075	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.5 A		13		S
Diode Forward Voltage ^b	V _{SD}	I _S = 2 A, V _{GS} = 0 V		0.9	1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.5 A		19	30	nC
Gate-Source Charge	Q _{gs}			4		
Gate-Drain Charge	Q _{gd}			3		
Gate Resistance	R _g		1		3.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		13	20	ns
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			36	60	
Fall Time	t _f			11	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs		35	60	

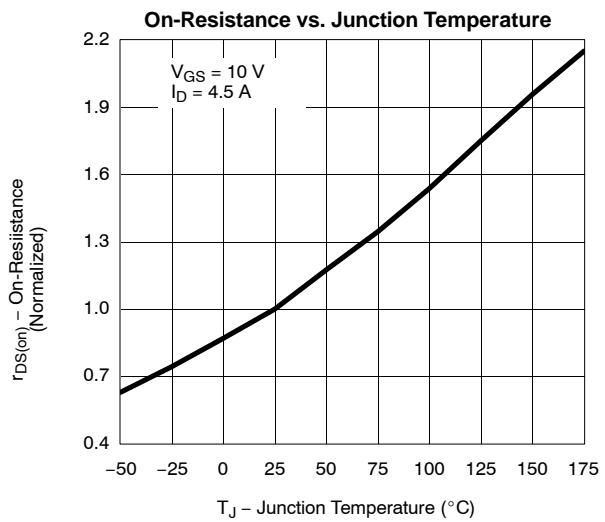
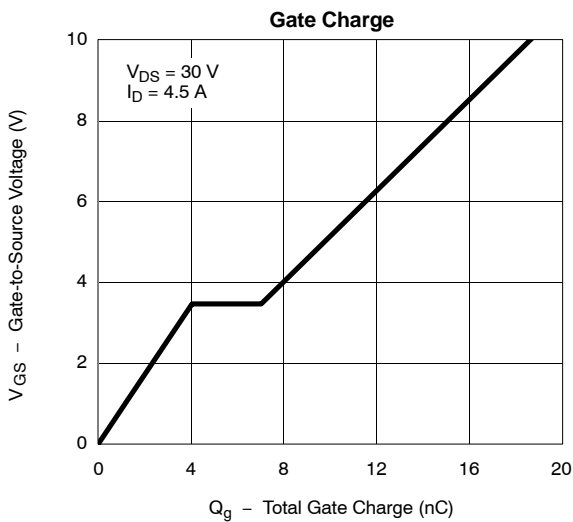
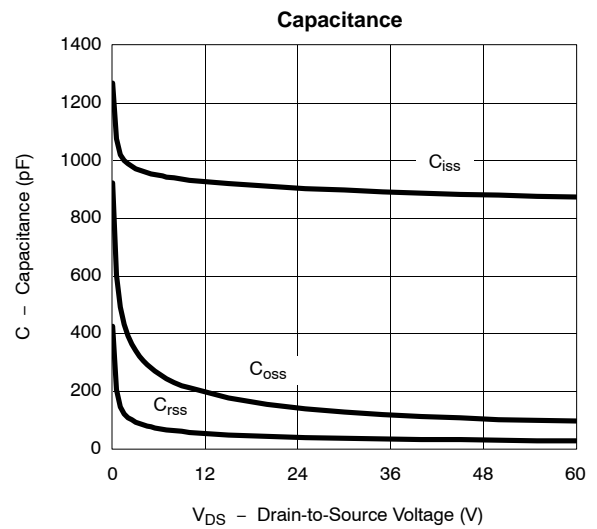
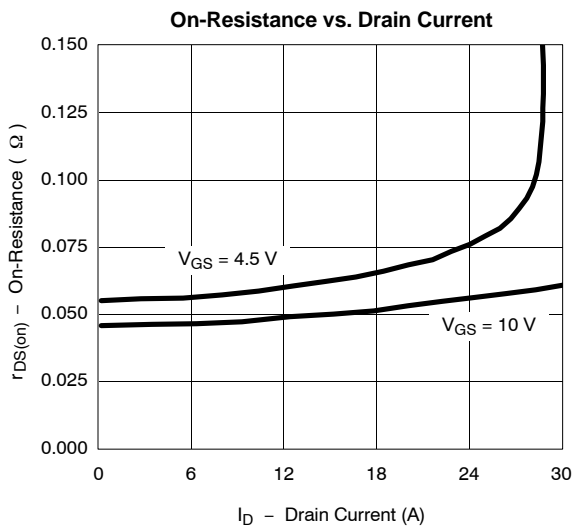
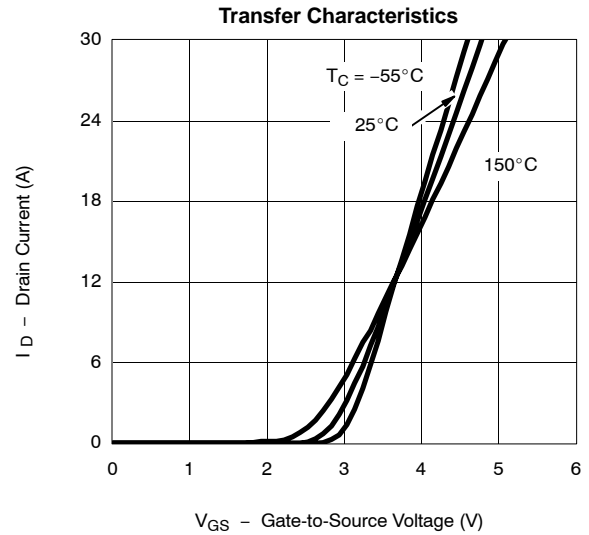
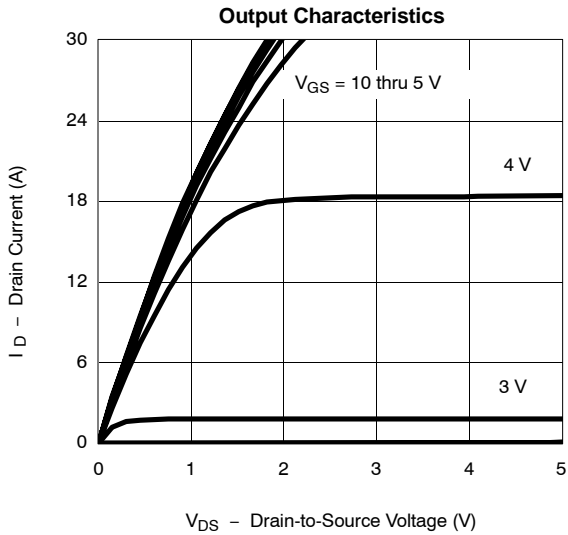
Notes

- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

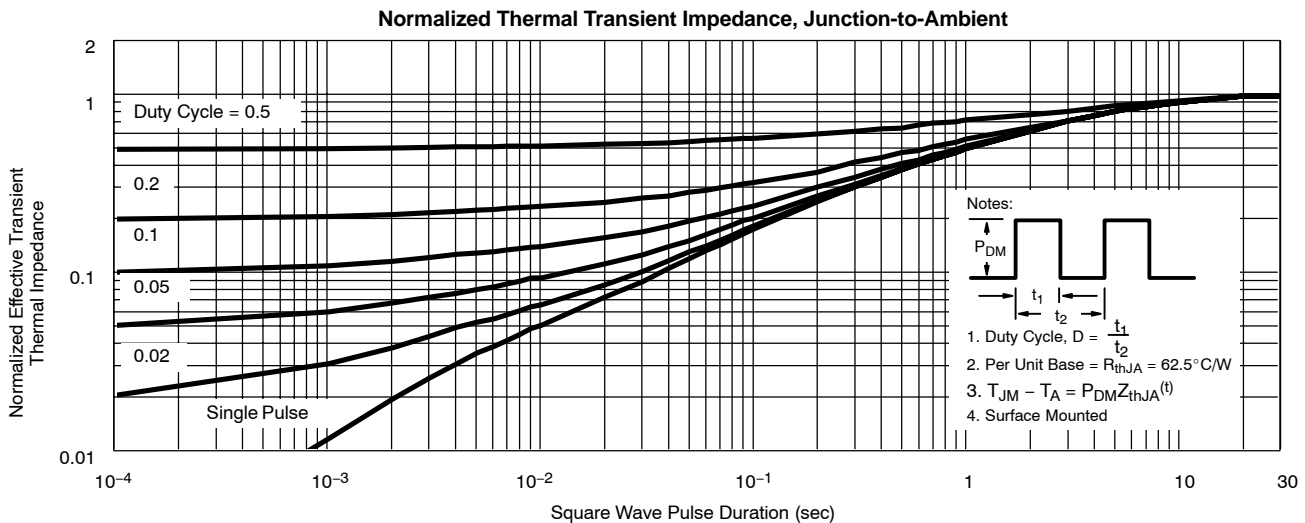
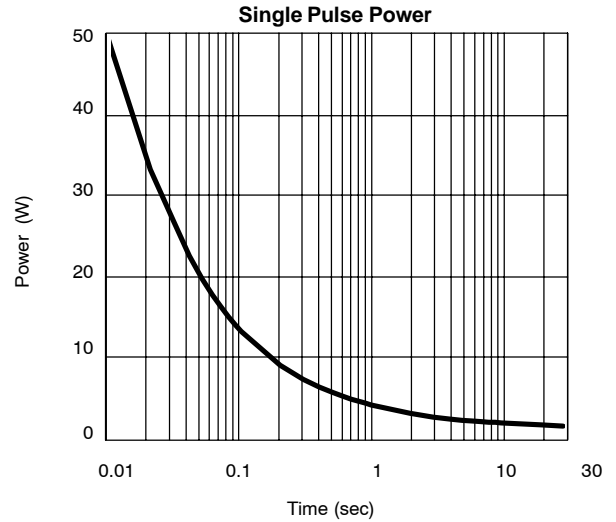
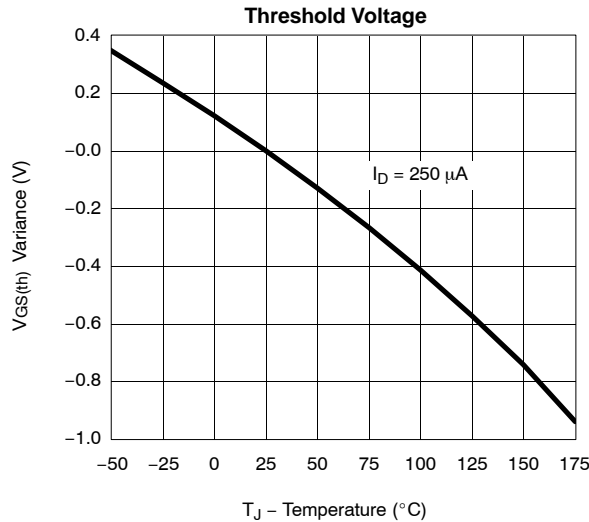
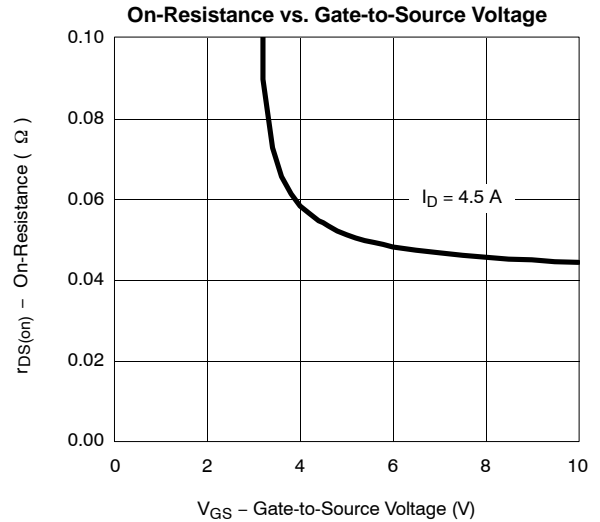
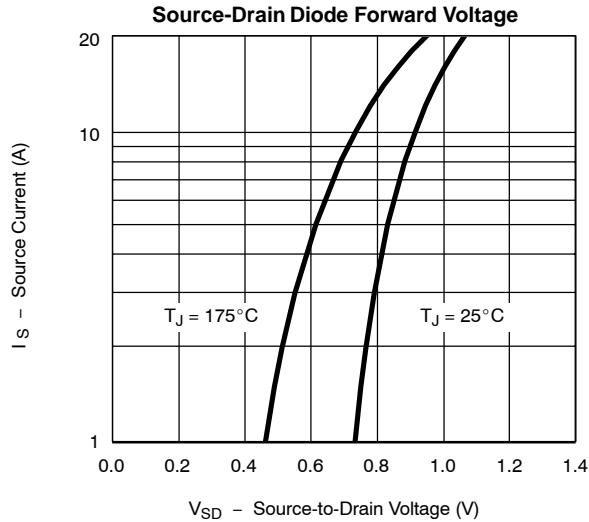


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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