SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs

- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle

- Overriding Clear Terminates Output Pulse

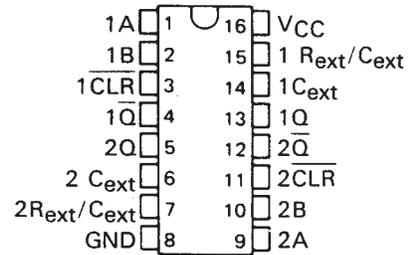- '122 and 'LS122 Have Internal Timing Resistors

description

These d-c triggered multivibrators feature output pulse-duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122 and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.
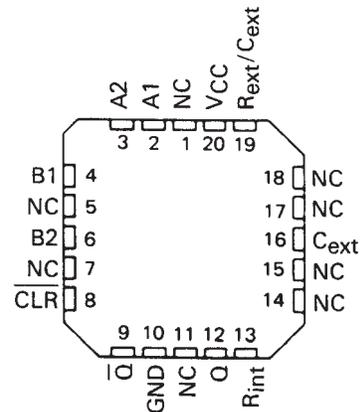
The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

The R_{int} in nominall 10 kΩ for '122 and 'LS122.

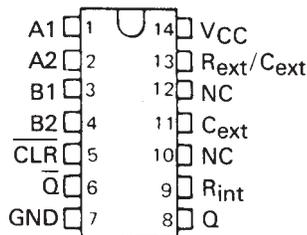**SN54122, SN54LS122 . . . J OR W PACKAGE**
SN74122 . . . N PACKAGE
SN74LS122 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

```
        A1  [ 1    14 ]  VCC
        A2  [ 2    13 ]  Rext/Cext
        B1  [ 3    12 ]  NC
        B2  [ 4    11 ]  Cext
       CLR  [ 5    10 ]  NC
         Q̄  [ 6     9 ]  Rint
       GND  [ 7     8 ]  Q
```

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse duration accuracy and repeatability, connect an external resistor between R_{ext}/Ce_{xt} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse durations, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

SN54123, SN54130, SN54LS123 . . . J OR W PACKAGE
SN74123, SN74130 . . . N PACKAGE
SN74LS123 . . . D OR N PACKAGE
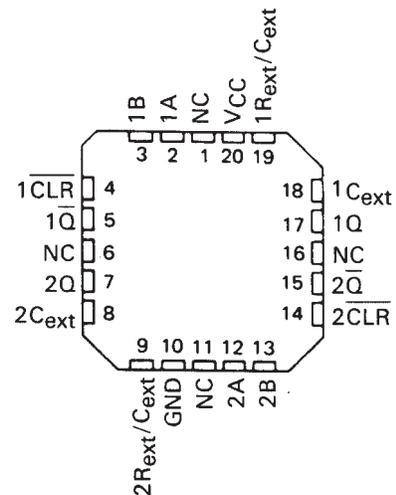**(TOP VIEW) (SEE NOTES 1 THRU 4)**

```
         1A  [ 1    16 ]  VCC
         1B  [ 2    15 ]  1 Rext/Cext
       1CLR  [ 3    14 ]  1Cext
         1Q̄  [ 4    13 ]  1Q
         2Q  [ 5    12 ]  2Q̄
      2 Cext [ 6    11 ]  2CLR
  2Rext/Cext [ 7    10 ]  2B
        GND  [ 8     9 ]  2A
```

SN54LS122 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

```
              A2  A1  NC  VCC  Rext/Cext
               3   2   1   20   19
        B1 [ 4                  18 ] NC
        NC [ 5                  17 ] NC
        B2 [ 6                  16 ] Cext
        NC [ 7                  15 ] NC
       CLR [ 8                  14 ] NC
               9  10  11  12  13
              Q̄  GND  NC   Q  Rint
```

SN54LS123 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

```
              1B  1A  NC  VCC  1Rext/Cext
               3   2   1   20   19
      1CLR [ 4                  18 ] 1Cext
        1Q̄ [ 5                  17 ] 1Q
        NC [ 6                  16 ] NC
        2Q [ 7                  15 ] 2Q̄
      2Cext [ 8                 14 ] 2CLR
               9  10  11  12  13
         2Rext/Cext  GND  NC  2A  2B
```

NC - No internal connection

TEXAS INSTRUMENTS

SN54122, SN54123, SN54130, SN54LS122, SN54LS123,
SN74122, SN74123, SN74130, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

description (continued)
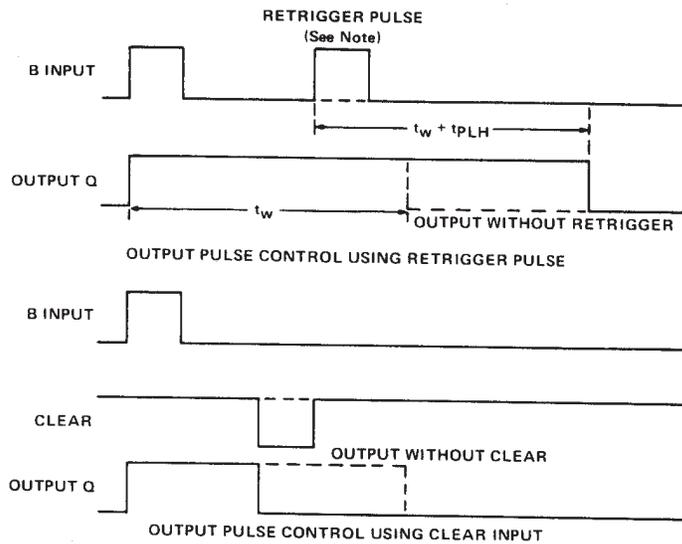
NOTE: Retrigger pulses starting before $0.22\,C_{ext}$ (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output duration will remain unchanged.

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

'122, 'LS122
FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⎍	⎐
H	L	X	H	↑	⎍	⎐
H	X	L	↑	H	⎍	⎐
H	X	L	H	↑	⎍	⎐
H	H	↓	H	H	⎍	⎐
H	↓	↓	H	H	⎍	⎐
H	↓	H	H	H	⎍	⎐
↑	L	X	H	H	⎍	⎐
↑	X	L	H	H	⎍	⎐

'123, '130, 'LS123
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎐
H	↓	H	⎍	⎐
↑	L	H	⎍	⎐

See explanation of function tables on page

† These lines of the functional tables assume that the indicated steady-state conditons at the A and B inputs have been set up long enough to complete any pulse started before the set up.
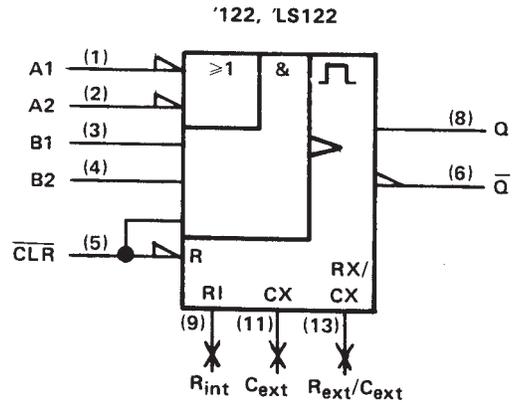
logic diagram (positive logic)

logic symbol†
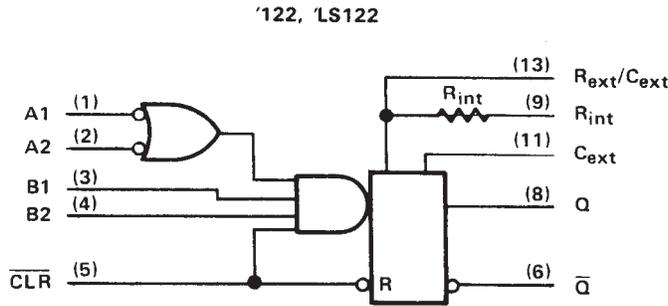
'122, 'LS122

R_{int} is nominally 10 kΩ for '122 and 'LS122

logic diagram (positive logic) (each multivibrator)

logic symbol†

'123, '130, 'LS123
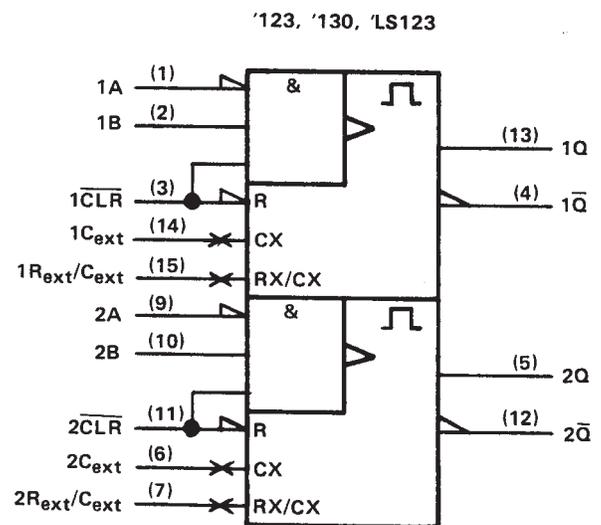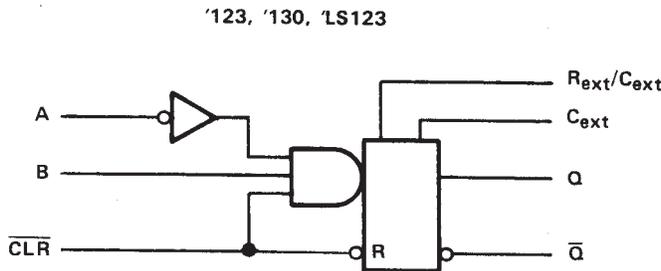
Pin numbers shown are for D, J, N, and W packages.

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs

'122, '123, '130 CIRCUITS

EQUIVALENT OF EACH INPUT

R_{eq}

Clear inputs : R_{eq} = 2 kΩ NOM
Other inputs : R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS

100 Ω NOM

'LS122, 'LS123 CIRCUITS

EQUIVALENT OF EACH INPUT

17 kΩ NOM

TYPICAL OF ALL OUTPUTS

120 Ω NOM
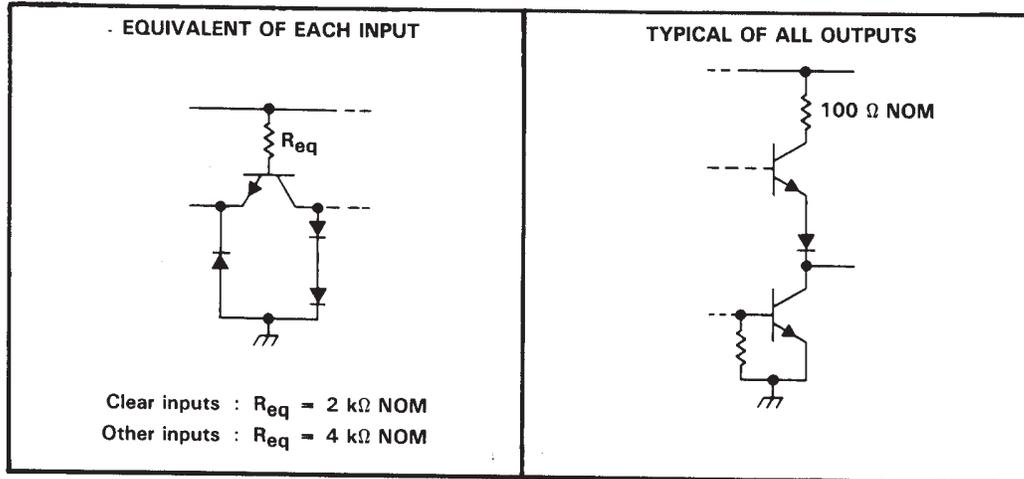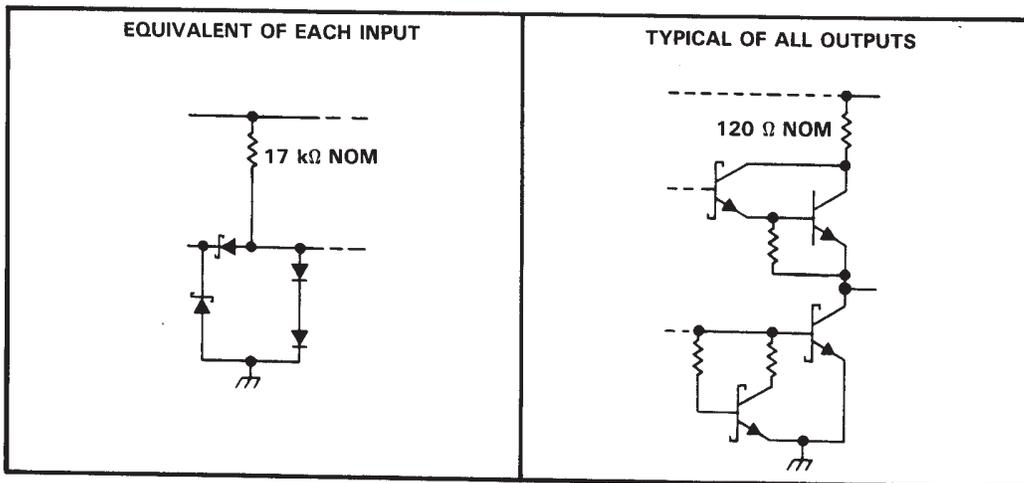
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: '122, '123, '130 . . . . 5.5 V
 'LS122, 'LS123 . . . . 7 V
Operating free-air temperature range: SN54' . . . . −55°C to 125°C
 SN74' . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54' MIN	SN54' NOM	SN54' MAX	SN74' MIN	SN74' NOM	SN74' MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Pulse duration, t_w	40			40			ns
External timing resistance, R_{ext}	5		25	5		50	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	'122 MIN	'122 TYP[‡]	'122 MAX	'123, '130 MIN	'123, '130 TYP[‡]	'123, '130 MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA, See Note 5	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA, See Note 5		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current — Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
	High-level input current — Clear input				80			80	
I_{IL}	Low-level input current — Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
	Low-level input current — Clear input				−3.2			−3.2	
I_{OS}	Short-circuit output current[§]	V_{CC} = MAX, See Note 5	−10		−40	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX, See Notes 6 and 7		23	36		46	66	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 4.5 V applied to all clear and A inputs, B inputs grounded, all outputs open and R_{ext} = 25 kΩ. R_{int} of '122 is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 8

PARAMETER[¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122, '130 MIN	'122, '130 TYP	'122, '130 MAX	'123 MIN	'123 TYP	'123 MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 400 Ω		22	33		22	33	ns
	B				19	28		19	28	
t_{PHL}	A	$\overline{Q}$			30	40		30	40	ns
	B				27	36		27	36	
t_{PHL}	Clear	Q			18	27		18	27	ns
t_{PLH}		$\overline{Q}$			30	40		30	40	
t_{wQ} (min)	A or B	Q			45	65		45	76	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω	3.08	3.42	3.76	2.76	3.03	3.37	μs

[¶] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{wQ} = duration of pulse at output Q.
NOTE 8: Load circuits and voltage waveforms are shown in Section 1.

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5

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse duration, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −400 μA	2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL}max	I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX, See Note 13	'LS122		6	11		6	11	mA
			'LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 12. To measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
        13. With all outputs open and 4.5 V applied to all data and clear inputs. I_{CC} is measured after a momentary ground, then 4.5 V, is applied to A or B inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 8)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	Q̄				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		Q̄				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶t_{PLH} = propagation delay time, low-to-high-level output
  t_{PHL} = propagation delay time, high-to-low-level output
  t_{wQ} = duration of pulse at output Q.
NOTE 8: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse durations when $C_{ext} \leq 1000$ pF, see Figure 4.

The output pulse duration is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse duration (t_W) is defined as:

$$t_W = K \cdot R_T \cdot C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

where

K is 0.32 for '122, 0.28 for '123 and '130

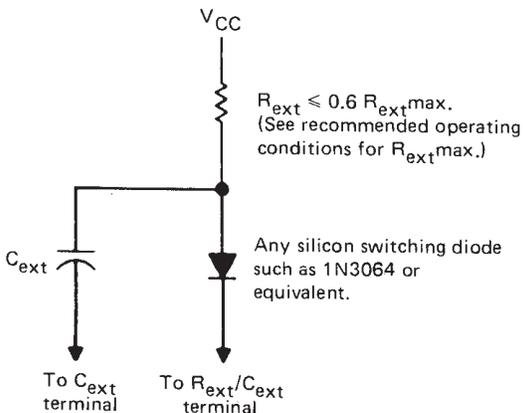R_T is in kΩ (internal or external timing resistance.)

C_{ext} is in pF

t_W is in ns

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse duration is:

$$t_W = K_D \cdot R_T \cdot C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

K_D is 0.28 for '122, 0.25 for '123 and '130

TIMING COMPONENT CONNECTIONS
FIGURE 3

TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE

FIGURE 4

† These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' circuits.
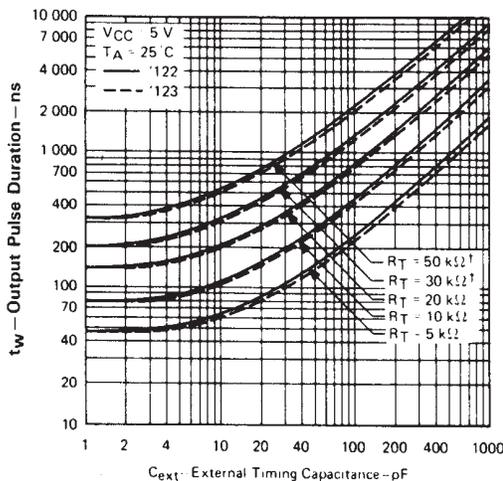

TIMING COMPONENT CONNECTIONS WHEN
$C_{ext} > 1000$ pF AND CLEAR IS USED
FIGURE 2

Applications requiring more precise pulse durations (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when $C_{ext} \leq 1000$ pF, use Figure 6, or use Figure 7 where the pulse duration may be defined as:

$$t_W = K \cdot R_T \cdot C_{ext}$$

When $C_{ext} \geq 1\ \mu F$, the output pulse width is defined as:

$$t_W = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

K is multiplier factor, see Figure 7
R_T is in kΩ (internal or external timing resistance)
C_{ext} is in pF
t_W is in ns

For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electolytic capacitors.

TIMING COMPONENT CONNECTIONS
FIGURE 5

'LS122, 'LS123
TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE
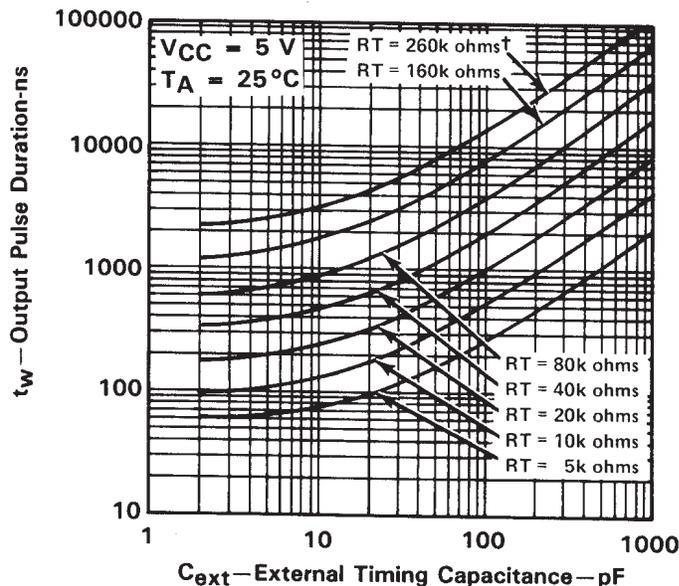
†This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 6

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123†

MULTIPLIER FACTOR
vs
EXTERNAL CAPACITOR

(K IS INDEPENDENT OF R)

C_{ext} – External Capacitor Value – uF

K – Multiplier Factor –

FIGURE 7

DISTRIBUTION OF UNITS
vs
OUTPUT PULSE DURATION

V_{CC} = 5 V
T_A = 25°C

Relative Frequency of Occurance

MEDIAN – 20%   MEDIAN + 20% – ('LS122)

See Note 14

– 8%   + 8% – ('LS122/ 'LS123)

|←—MEDIAN—→|98% OF UNITS

$t_{w(out)}$ – Output Pulse Duration
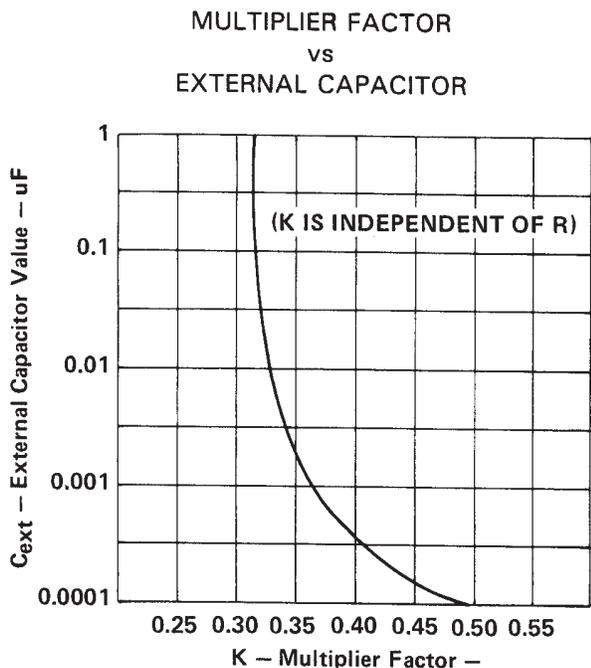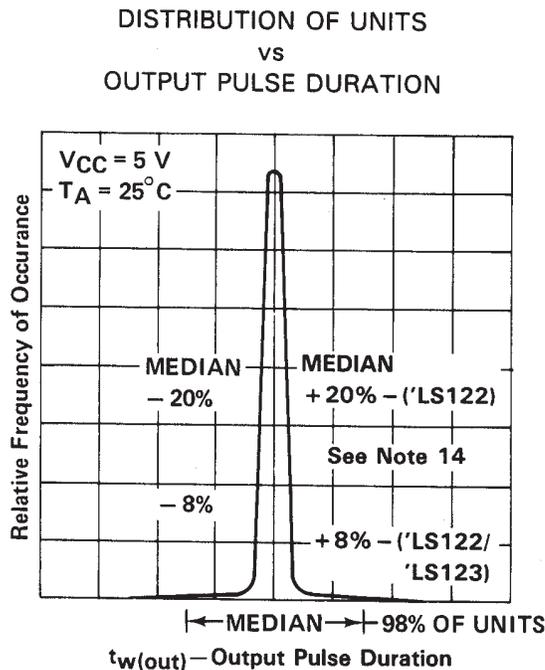
FIGURE 8

VARIATION IN OUTPUT PULSE DURATION
vs
SUPPLY VOLTAGE

$\Delta t_{w(out)}$ – Variation in Output Pulse Duration

C_{ext} = 60 pF
R_{ext} = 10 K ohms
T_A = 25°C

$t_{w(out)} \approx 370$ ns
at V_{CC} = 5 V

V_{CC} – Supply Voltage – V
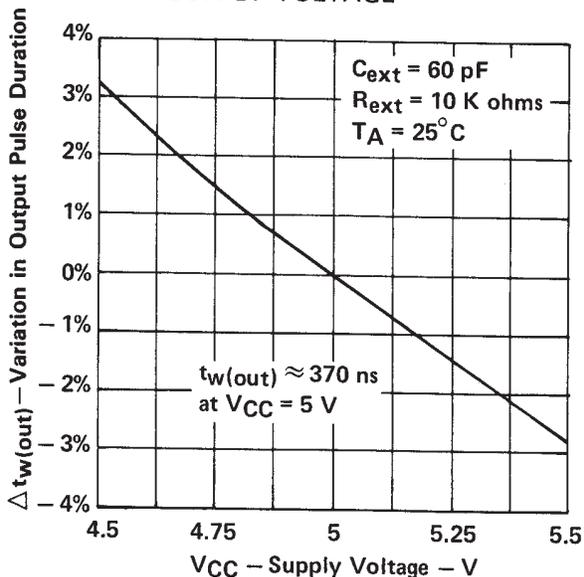
FIGURE 9

VARIATION IN OUTPUT PULSE DURATION
vs
FREE-AIR TEMPERATURE

$\Delta t_{w(out)}$ – Variation in Output Pulse Duration

V_{CC} = 5 V
C_{ext} = 60 pF
R_T = 10 K ohms

'LS122

$t_{w(out)} \approx 370$ ns
at T_A = 25°C

'LS122/'LS123
See Note 14

T_A – FREE-AIR TEMPERATURE – °C

FIGURE 10

NOTE 14: For the 'LS122, the internal timing resistor, R_{int} was used. For the 'LS122/123, an external timing resistor was used for R_T.
†Data for temperatures below 0°C and above 70°C and for suply voltages below 4.75 V and above 5.25 V are applicable for SN54LS122 and SN54LS123 only.

PACKAGING INFORMATION

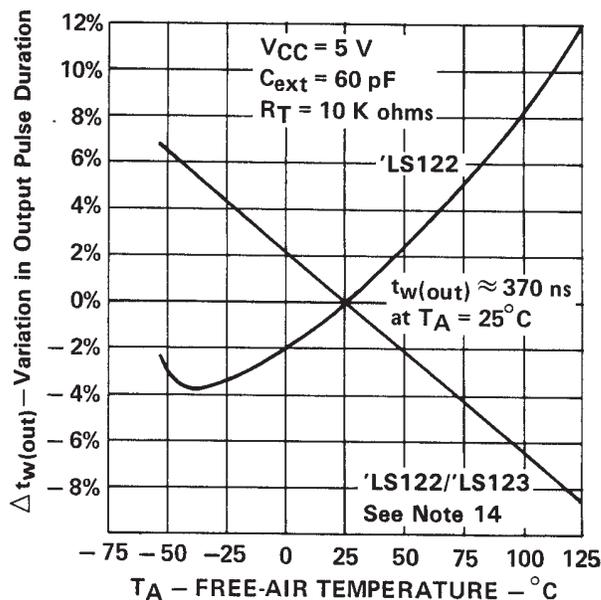| Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-7603901VEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7603901VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7603901EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7603901FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/01203BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/31401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/31401BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/31401BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54122J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54123J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS123J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74122N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74123N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74123N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74123NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS122D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS122DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS122DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS122DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS122N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS122N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS122NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS122NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS122NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LS123N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS123N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS123NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS123NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS123NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54122J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54123J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54123W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS123FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS123J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS123W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

C

1   7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R–GDFP–F16)　　　　　　　　　CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.285\ (7,24)}{0.245\ (6,22)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

$\dfrac{0.080\ (2,03)}{0.055\ (1,40)}$

0.305 (7,75) MAX

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

1

16

$\dfrac{0.430\ (10,92)}{0.370\ (9,40)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8

9

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$
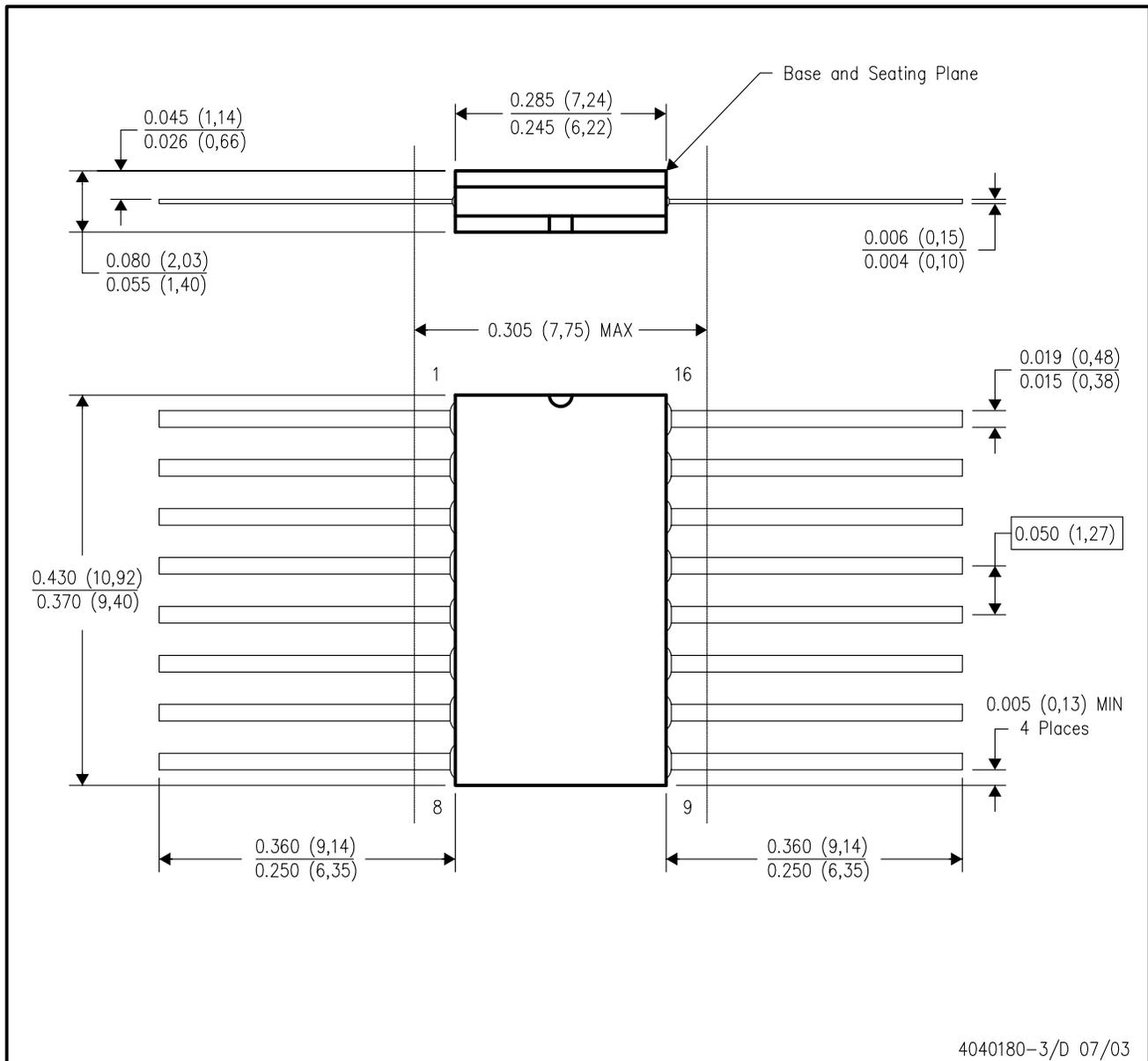
$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

4040180–3/D 07/03

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　This package can be hermetically sealed with a ceramic lid using glass frit.
　　　　　D.　Index point is provided on cap for terminal identification only.
　　　　　E.　Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

FK (S-CQCC-N)**   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

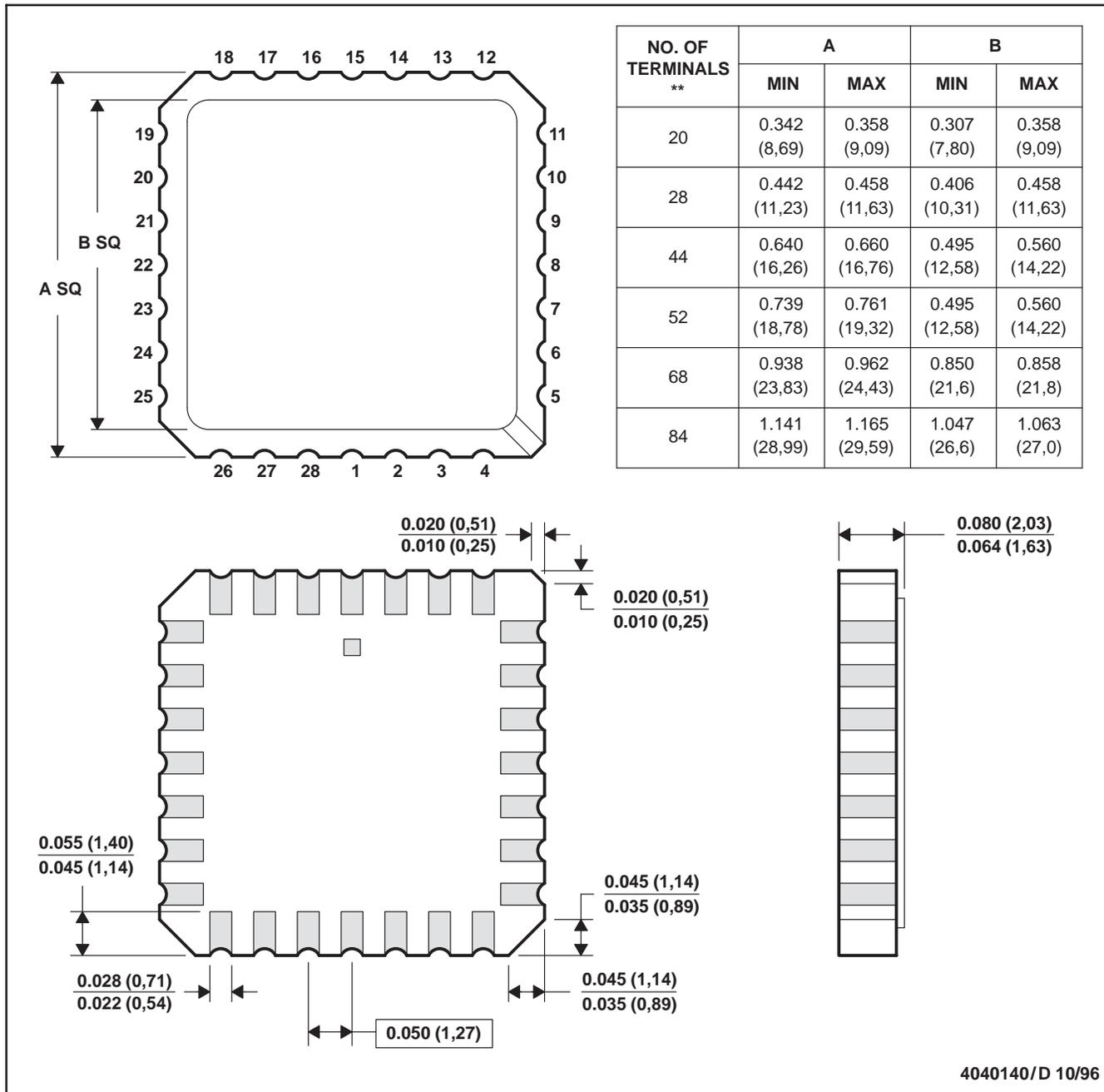0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. This package can be hermetically sealed with a metal lid.
   D. The terminals are gold plated.
   E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
⚠C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) ⚠D

0.045 (1,14)
0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002
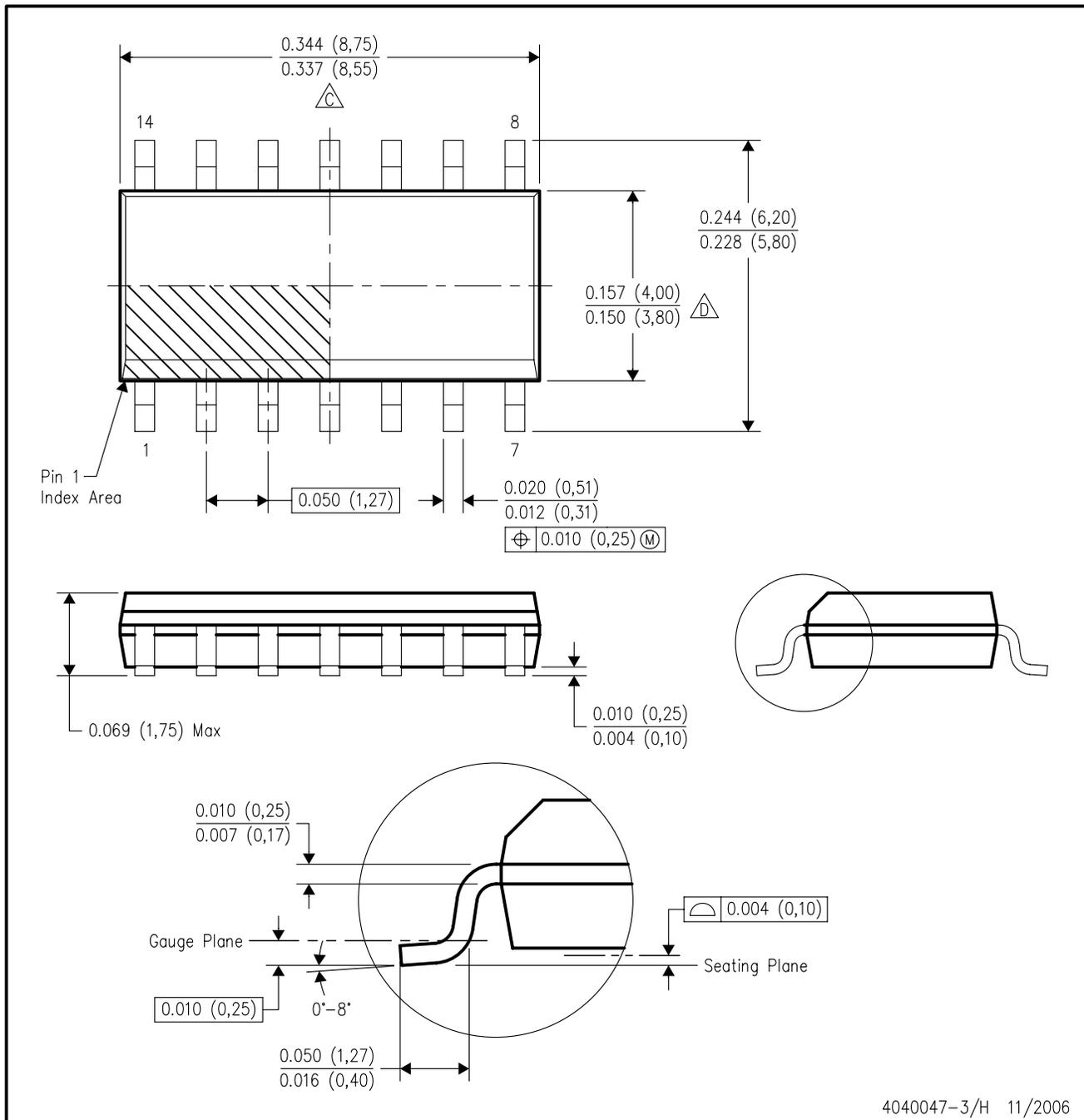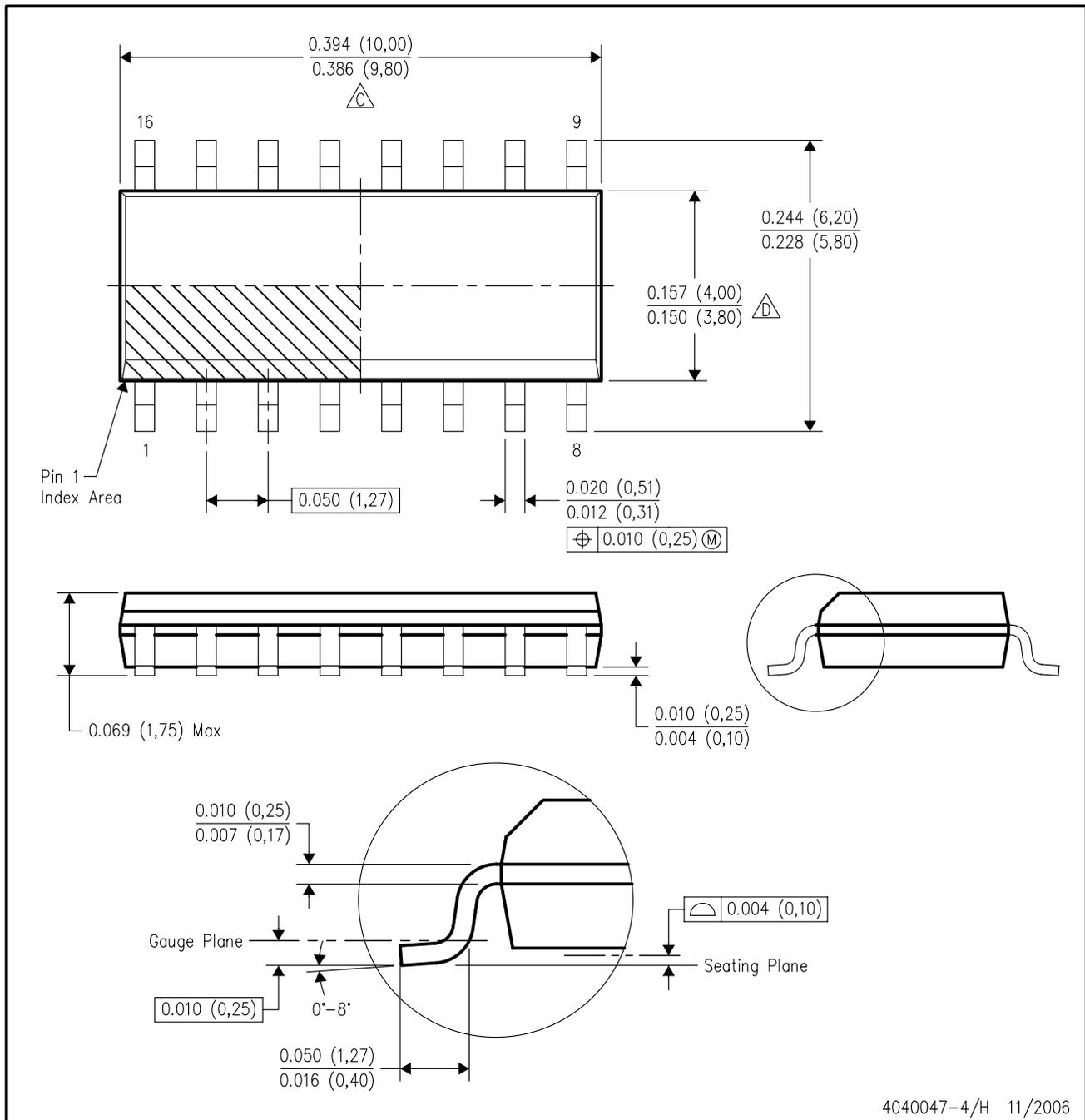
NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
        ⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        ⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)
⟨C⟩

14

8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1

7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) (M)

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

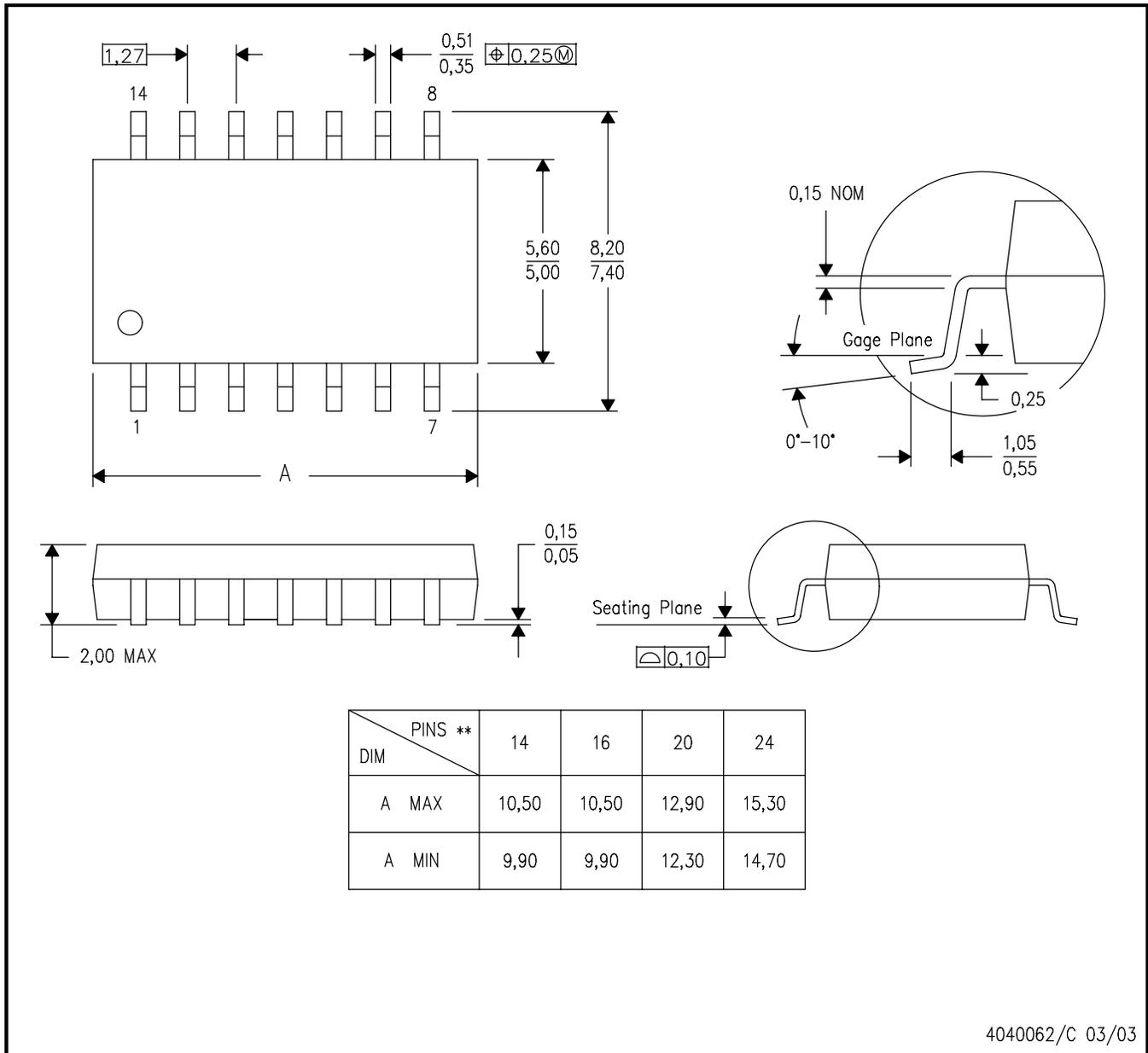0.050 (1,27)
0.016 (0,40)

4040047−3/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
    ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
         not exceed .006 (0,15) per end.
    ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E. Reference JEDEC MS−012 variation AB.

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D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

0.010 (0,25)   0°−8°

Seating Plane

0.050 (1,27)
0.016 (0,40)

4040047−4/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
     ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed .006 (0,15) per end.
     ⚠D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
        E. Reference JEDEC MS−012 variation AC.

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MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

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