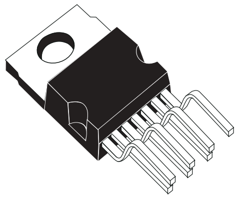
STV9302B

Vertical Deflection Booster for 2-App TV (50-60 Hz) Applications with 70-V Flyback Generator

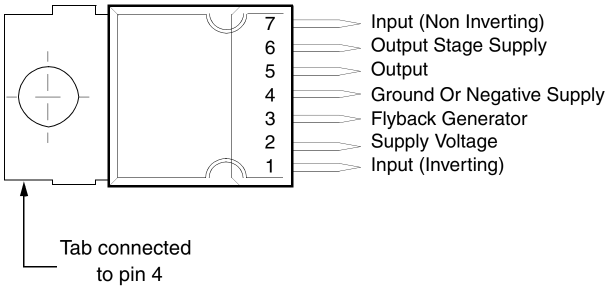
DATASHEET

Main Features

- **Power Amplifier**
- **Flyback Generator**
- **Output Current up to 2 App**
- **Thermal Protection**



HEPTAWATT
(Plastic Package)
ORDER CODE: STV9302B

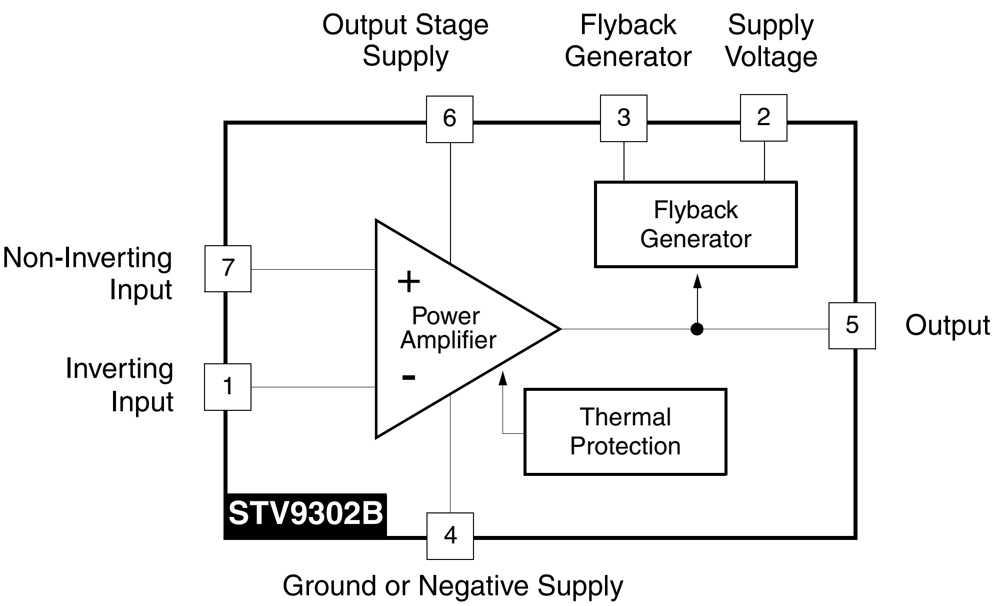


Description

The STV9302B is a vertical deflection booster designed for TV (50-60 Hz) applications.

This device, supplied with up to 35 V, provides up to 2 App output current to drive the vertical deflection yoke.

The internal flyback generator delivers flyback voltages up to 70 V.



1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Voltage			
V_S	Supply Voltage (pin 2) - Note 1 and Note 2	40	V
V_5, V_6	Flyback Peak Voltage - Note 2	70	V
V_3	Voltage at Pin 3 - Note 2, Note 3 and Note 6	-0.4 to (V_S + 3)	V
V_1, V_7	Amplifier Input Voltage - Note 2, Note 6 and Note 7	- 0.4 to (V_S + 2) or +40	V
Current			
I_0 (1)	Output Peak Current at f = 50 to 65 Hz, t ≤10 µs - Note 4	±5	A
I_0 (2)	Output Peak Current non-repetitive - Note 5	±2	A
$I_{3\ Sink}$	Sink Current, t < 1 ms - Note 3	1.5	A
$I_{3\ Source}$	Source Current, t < 1 ms	1.5	A
I_3	Flyback pulse current at f = 50 to 65 Hz, t ≤10 µs - Note 4	±5	A
ESD Susceptibility			
ESD1	Human body model (100 pF discharged through 1.5 kΩ)	2	kV
ESD2	EIAJ Standard (200 pF discharged through 0 Ω)	300	V
Temperature			
T_s	Storage Temperature	-40 to 150	°C
T_j	Junction Temperature	+150	°C

Note:1. Usually the flyback voltage is slightly more than 2 x V_S. This must be taken into consideration when setting V_S.

2. Versus pin 4

3. V3 is higher than V_S during the first half of the flyback pulse.

4. Such repetitive output peak currents are usually observed just before and after the flyback pulse.

5. This non-repetitive output peak current can be observed, for example, during the Switch-On/Switch-Off phases. This peak current is acceptable providing the SOA is respected (Figure 8 and Figure 9).

6. All pins have a reverse diode towards pin 4, these diodes should never be forward-biased.

7. Input voltages must not exceed the lower value of either V_S + 2 or 40 volts.

2 Thermal Data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-to-Case Thermal Resistance	3	°C/W
T_T	Temperature for Thermal Shutdown	150	°C
T_J	Recommended Max. Junction Temperature	120	°C

3 Electrical Characteristics

(V_S = 32 V, T_{AMB} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
Supply							
V_S	Operating Supply Voltage Range (V_2-V_4)	Note 8	10		35	V	
I_2	Pin 2 Quiescent Current	I_3 = 0, I_5 = 0		5	20	mA	1
I_6	Pin 6 Quiescent Current	I_3 = 0, I_5 = 0, V_6 =35v	8	19	50	mA	1
Input							
I_1	Input Bias Current	V_1 = 1 V, V_7 = 2.2 V		- 0.6	-1.5	µA	1
I_7	Input Bias Current	V_1 = 2.2 V, V_7 = 1 V		- 0.6	-1.5	µA	
V_{IR}	Operating Input Voltage Range		0		V_S - 2	V	
V_{I0}	Offset Voltage			2		mV	
$\Delta V_{I0}/dt$	Offset Drift versus Temperature			10		µV/°C	
Output							
I_0	Operating Peak Output Current	f = 50 to 60 Hz			±1	A	
V_{5L}	Output Saturation Voltage to pin 4	I_5 = 1 A		1	1.7	V	3
V_{5H}	Output Saturation Voltage to pin 6	I_5 = -1 A		1.8	2.3	V	2
Miscellaneous							
G	Voltage Gain		80			dB	
V_{D5-6}	Diode Forward Voltage Between pins 5-6	I_5 = 1 A		1.4	2	V	
V_{D3-2}	Diode Forward Voltage between pins 3-2	I_3 = 1 A		1.3	2	V	
V_{3SL}	Saturation Voltage on pin 3	I_3 = 20 mA		0.4	1	V	3
V_{3SH}	Saturation Voltage to pin 2 (2nd part of flyback)	I_3 = -1 A		2.1		V	

8. *In normal applications, the peak flyback voltage is slightly greater than 2 x (V_S - V_4). Therefore, (V_S - V_4) = 35 V is not allowed without special circuitry.*

Figure 1: Measurement of I_1, I_2 and I_6

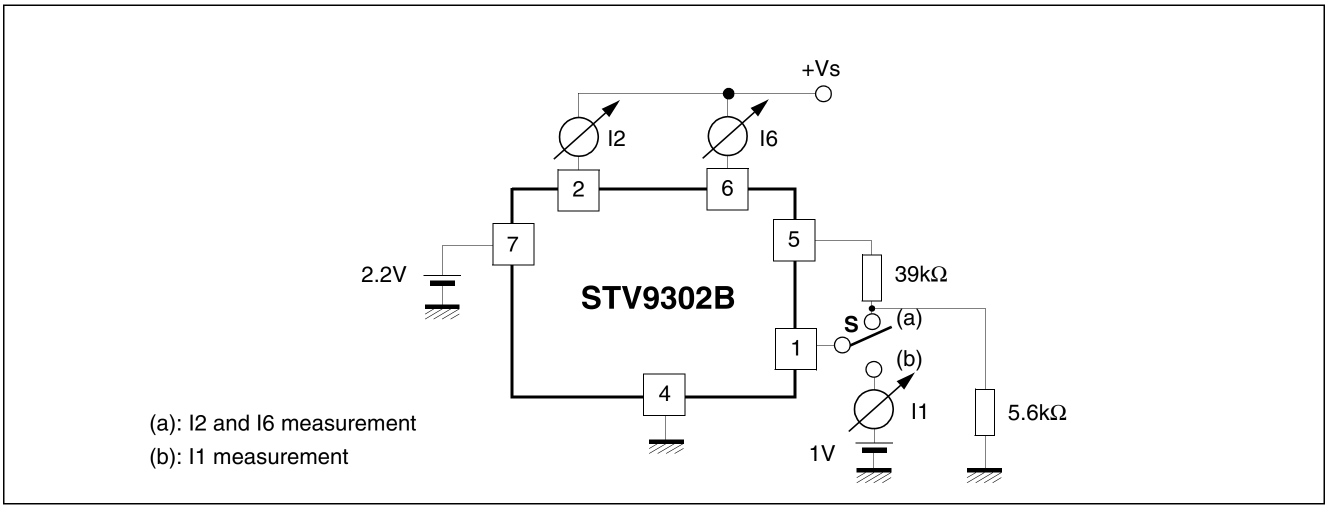


Figure 2: Measurement of V_{5H}

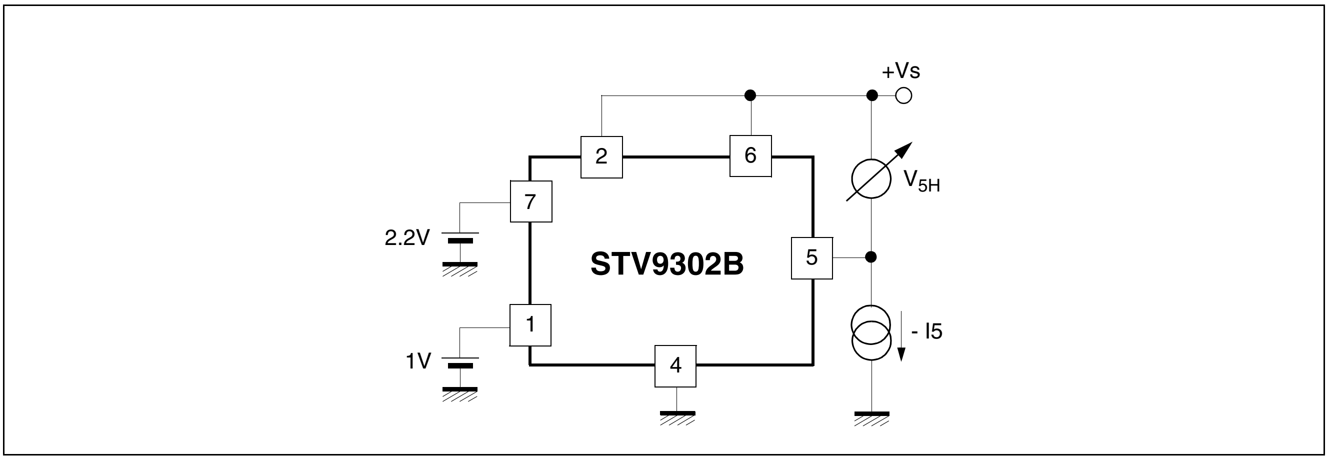
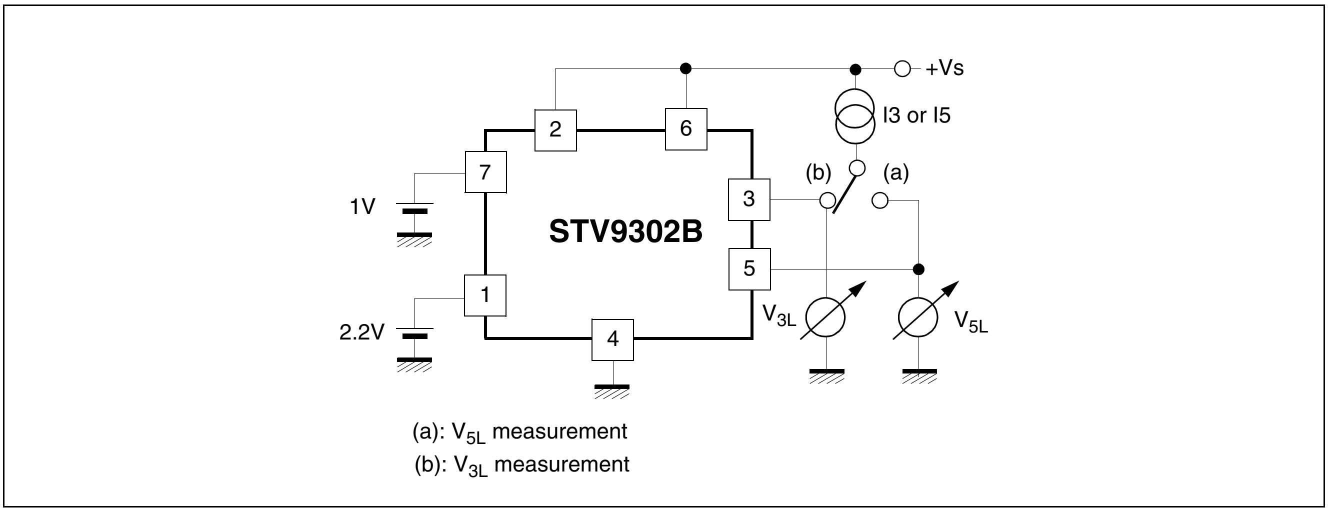


Figure 3: Measurement of V_{3L} and V_{5L}



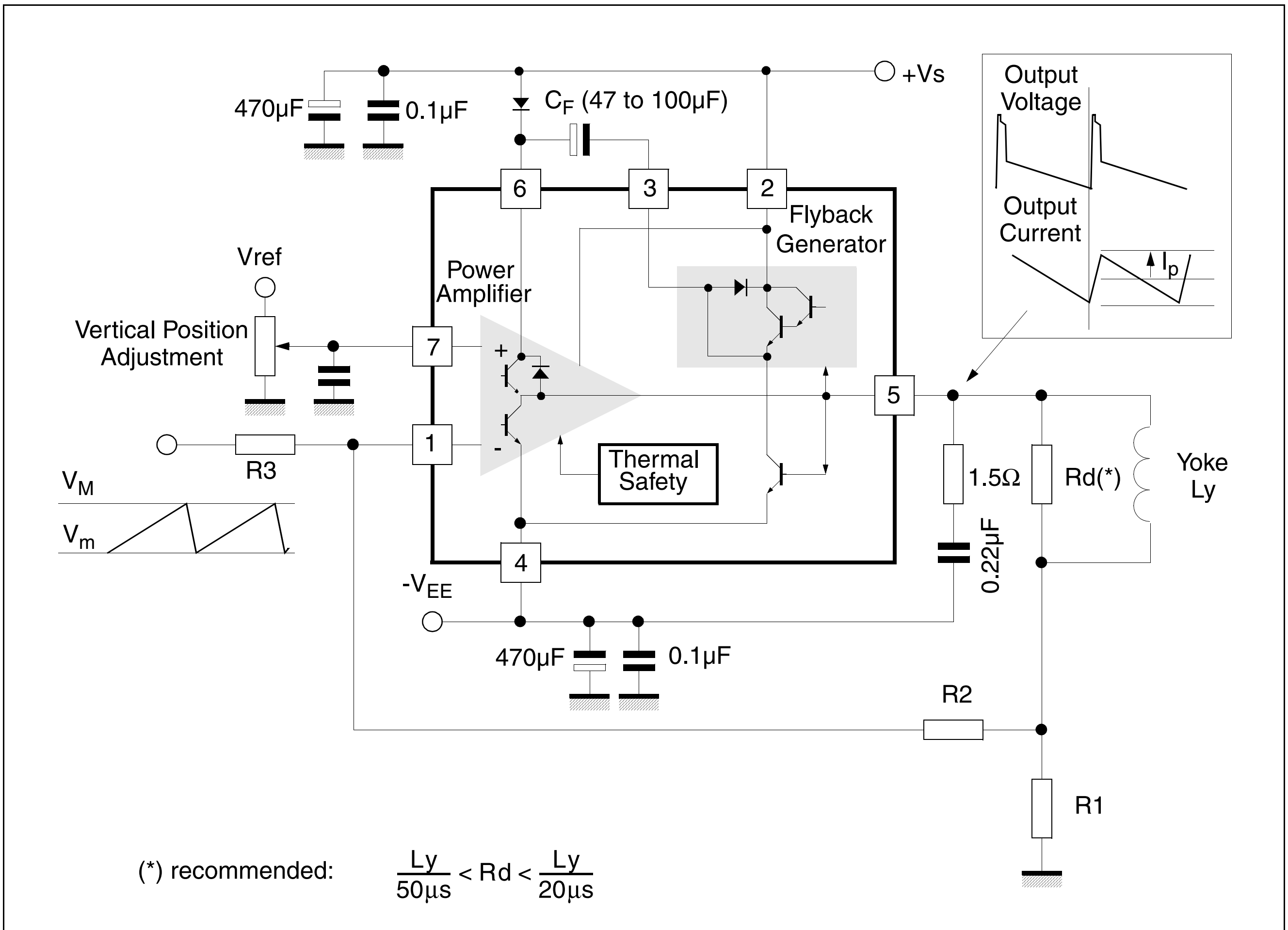
4 Application Hints

The yoke can be coupled either in AC or DC.

4.1 DC-coupled Application

When DC coupled (see Figure 4), the display vertical position can be adjusted with input bias. On the other hand, 2 supply sources (V_S and $-V_{EE}$) are required.

Figure 4: DC-coupled Application



4.1.1 Application Hints

For calculations, treat the IC as an op-amp, where the feedback loop maintains $V_1 = V_7$.

4.1.1.1 Centering

Display will be centered (null mean current in yoke) when voltage on pin 7 is (R_1 is negligible):

$$V_7 = \frac{V_M + V_m}{2} \times \left(\frac{R_2}{R_2 + R_3}\right)$$

4.1.1.2 Peak Current

$$I_P = \frac{(V_M - V_m)}{2} \times \frac{R_2}{R_1 x R_3}$$

Example: for $V_m = 2$ V, $V_M = 5$ V and $I_P = 1$ A

Choose R_1 in the1 Ω range, for instance R_1=1 Ω

From equation of peak current: $\frac{R_2}{R_3} = \frac{2 \times I_P \times R_1}{V_M - V_m} = \frac{2}{3}$

Then choose R_2 or R_3. For instance, if R_2 = 10 kΩ, then R_3 = 15 kΩ

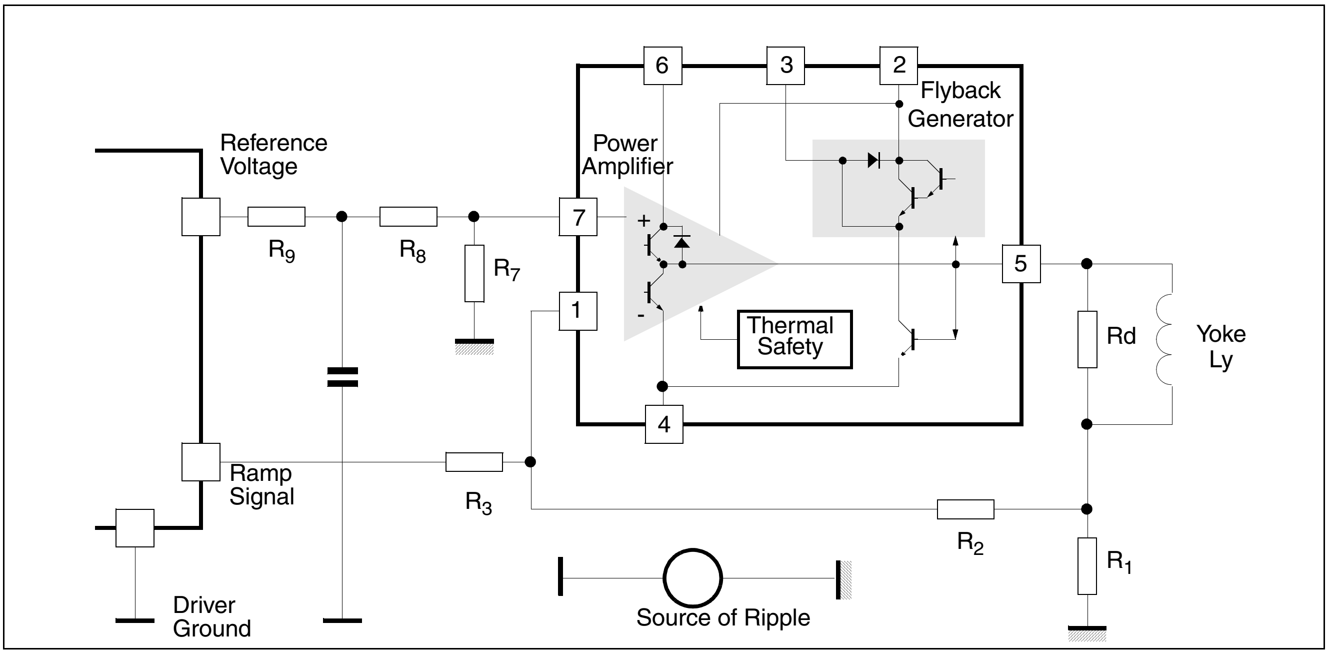
Finally, the bias voltage on pin 7 should be:

$$V_7 = \frac{V_M + V_m}{2} \times \frac{1}{1 + \frac{R_3}{R_2}} = \frac{7}{2} \times \frac{1}{2.5} = 1.4V$$

4.1.2 Ripple Rejection

When both ramp signal and bias are provided by the same driver IC, you can gain natural rejection of any ripple caused by a voltage drop in the ground (see Figure 5), if you manage to apply the same fraction of ripple voltage to both booster inputs. For that purpose, arrange an intermediate point in the bias resistor bridge, such that (R_8 / R_7) = (R_3 / R_2), and connect the bias filtering capacitor between the intermediate point and the local driver ground. Of course, R_7 should be connected to the booster reference point, which is the ground side of R_1.

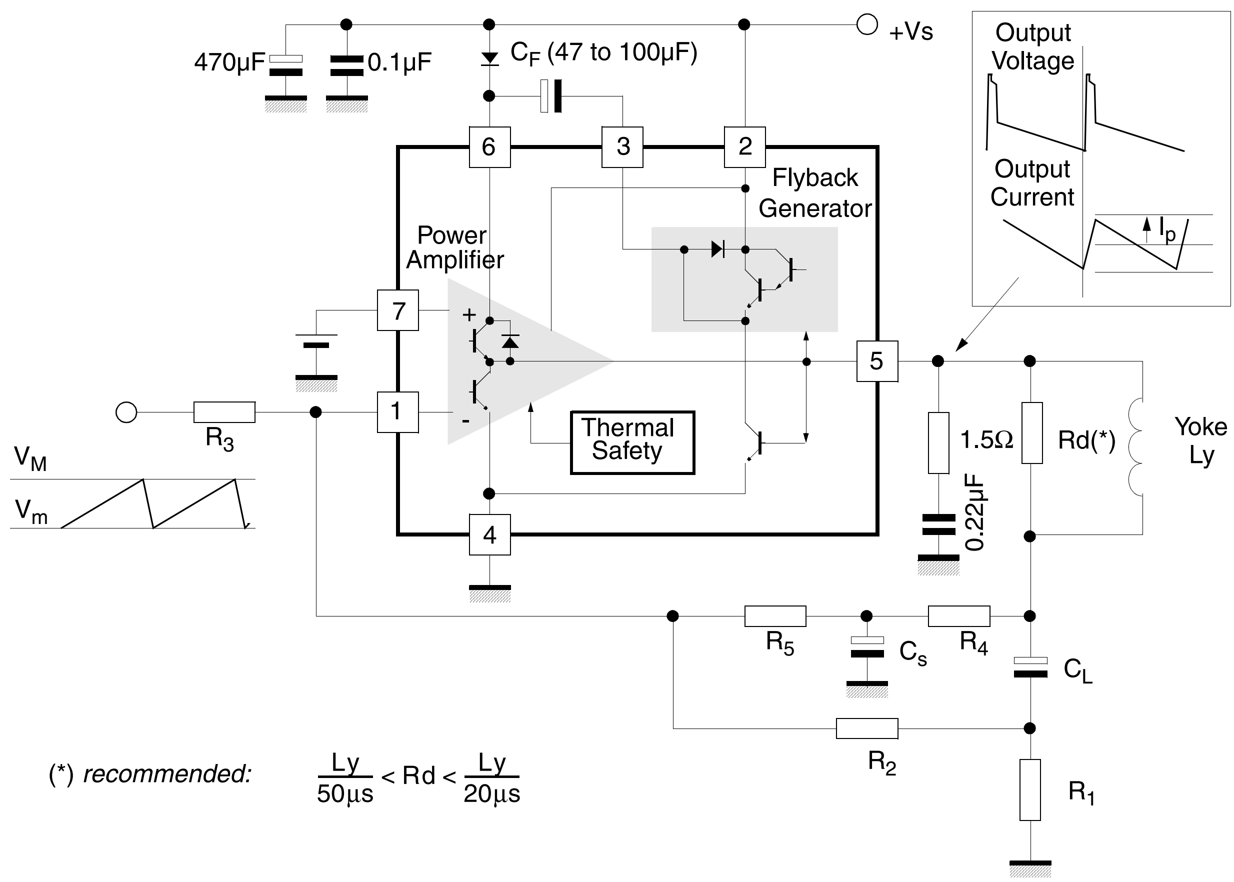
Figure 5: Ripple Rejection



4.2 AC-Coupled Applications

In AC-coupled applications (See Figure 6), only one supply (V_S) is needed. The vertical position of the scanning cannot be adjusted with input bias (for that purpose, usually some current is injected or sunk with a resistor in the low side of the yoke).

Figure 6: AC-coupled Application



(*) *recommended:* $\frac{Ly}{50\mu s} < Rd < \frac{Ly}{20\mu s}$

4.2.1 Application Hints

Gain is defined as in the previous case:

$$I_p = \frac{V_M - V_m}{2} \times \frac{R_2}{R_1 \times R_3}$$

Choose R_1 then either R_2 or R_3. For good output centering, V_7 must fulfill the following equation:

$$\frac{\frac{V_S}{2} - V_7}{R_4 + R_5} = \frac{V_7 - \frac{V_M + V_m}{2}}{R_3} + \frac{V_7}{R_2}$$

or

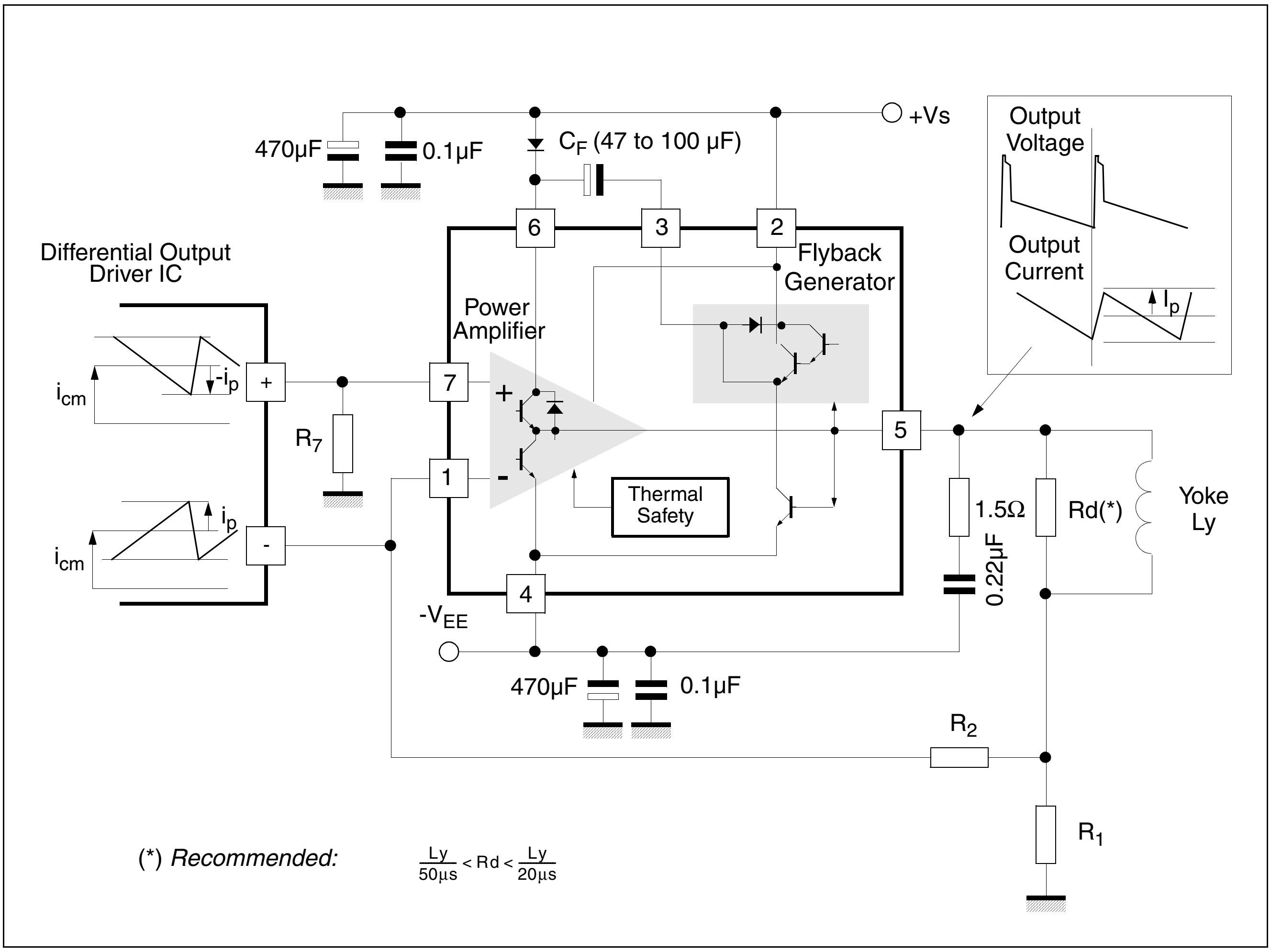
$$V_7 \times \left(\frac{1}{R_3} + \frac{1}{R_2} + \frac{1}{R_4 + R_5}\right) = \left(\frac{V_S}{2(R_4 + R_5)} + \frac{V_M + V_m}{2 \times R_3}\right)$$

C_S performs an integration of the parabolic signal on C_L, therefore the amount of S correction is set by the combination of C_L and C_s.

4.3 Application with Differential-output Drivers

Certain driver ICs provide the ramp signal in differential form, as two current sources i_+ and $i_$with opposite variations.

Figure 7: Using a Differential-output Driver



Let us set some definitions:

- i_{cm} is the common-mode current: $i_{cm} = \frac{1}{2}(i_+ + i_-)$
- at peak of signal, $i_+ = i_{cm} + i_p$ and $i\_= i_{cm} - i_p$, therefore the peak differential signal is $i_p - (-i_p) = 2\, i_p$, and the peak-peak differential signal, $4i_p$.

The application is described in Figure 7 with DC yoke coupling. The calculations still rely on the fact that V_1 remains equal to V_7.

4.3.1 Centering

When idle, both driver outputs provide i_{cm} and the yoke current should be null (R_1 is negligible), hence:

$$i_{cm} \cdot R_7 = i_{cm} \cdot R_2 \quad \text{therefore} \quad R_7 = R_2$$

4.3.2 Peak Current

Scanning current should be I_P when positive and negative driver outputs provide respectively i_{cm} - i_p and i_{cm} + i_p, therefore

$$(i_{cm} - i) \cdot R_7 = I_p \cdot R_1 + (i_{cm} + i) \cdot R_2 \quad \text{and since } R_7 = R_2\text{:} \quad \frac{I_p}{i} = -\frac{2R_7}{R_1}$$

Choose R_1 in the 1Ω range, the value of $R_2 = R_7$ follows. Remember that i is one-quarter of driver peak-peak differential signal! Also check that the voltages on the driver outputs remain inside allowed range.

- Example: for i_{cm} = 0.4mA, i = 0.2mA (corresponding to 0.8mA of peak-peak differential current), I_p = 1A

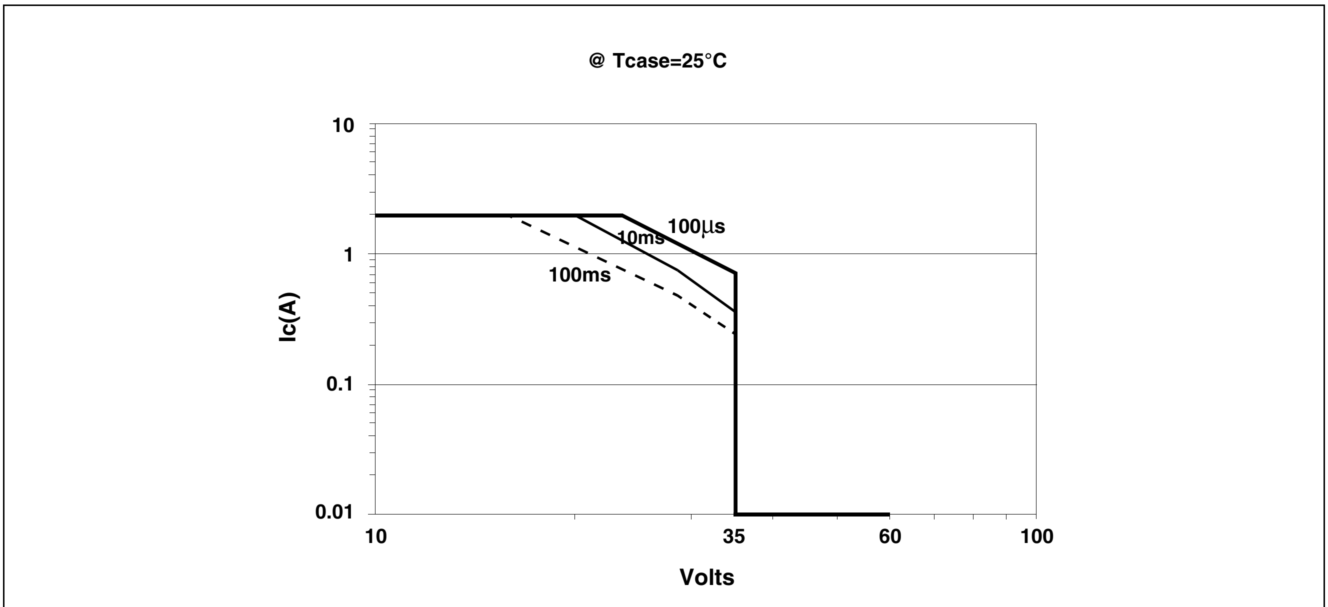
  Choose R_1 = 0.75Ω, it follows $R_2 = R_7$ = 1.875kΩ

4.3.3 Ripple Rejection

Make sure to connect R_7 directly to the ground side of R_1.

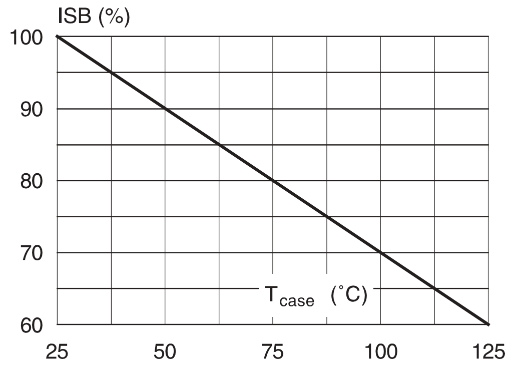
4.3.4 Secondary Breakdown Diagrams

Figure 8: Output Transistor Safe Operating Area (SOA) for Secondary Breakdown



The diagram has been arbitrarily limited to max VS (35 V) and max I0 (2 A).

Figure 9: Secondary Breakdown Temperature Derating Curve (ISB = Secondary Breakdown Current)



4.4 Horizontal Noise Reduction

If the level of the noise induced in the vertical deflection yoke by the horizontal deflection yoke must be reduced, a capacitor should be added in parallel with the vertical deflection yoke.

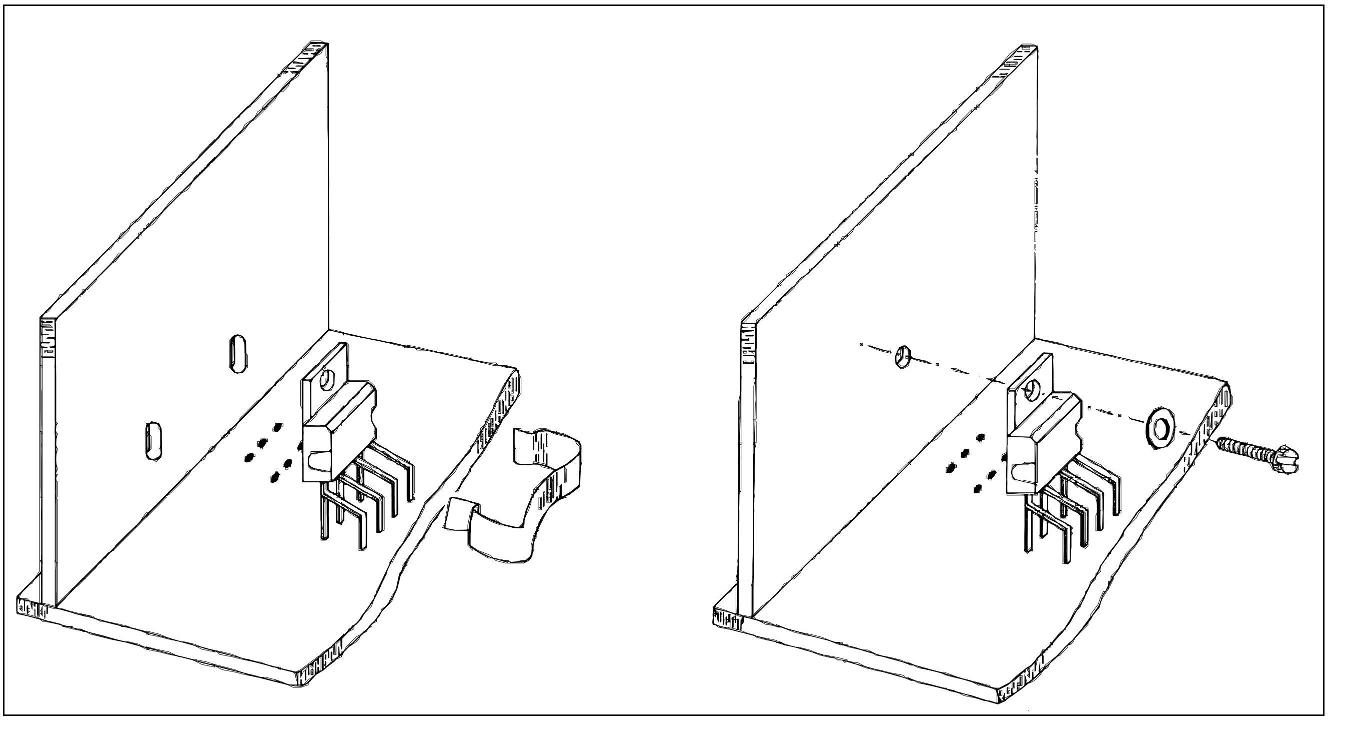
In this case the maximum recommended value of the capacitor is 100 nF.

5 Mounting Instructions

The power dissipated in the circuit is removed by adding an external heatsink. With the HEPTAWATT™ package, the heatsink is simply attached with a screw or a compression spring (clip).

A layer of silicon grease inserted between heatsink and package optimizes thermal contact. In DC-coupled applications we recommend to use a silicone tape between the device tab and the heatsink to electrically isolate the tab.

Figure 10: Mounting Examples



6 Pin Configuration

Figure 11: Pins 1 and 7

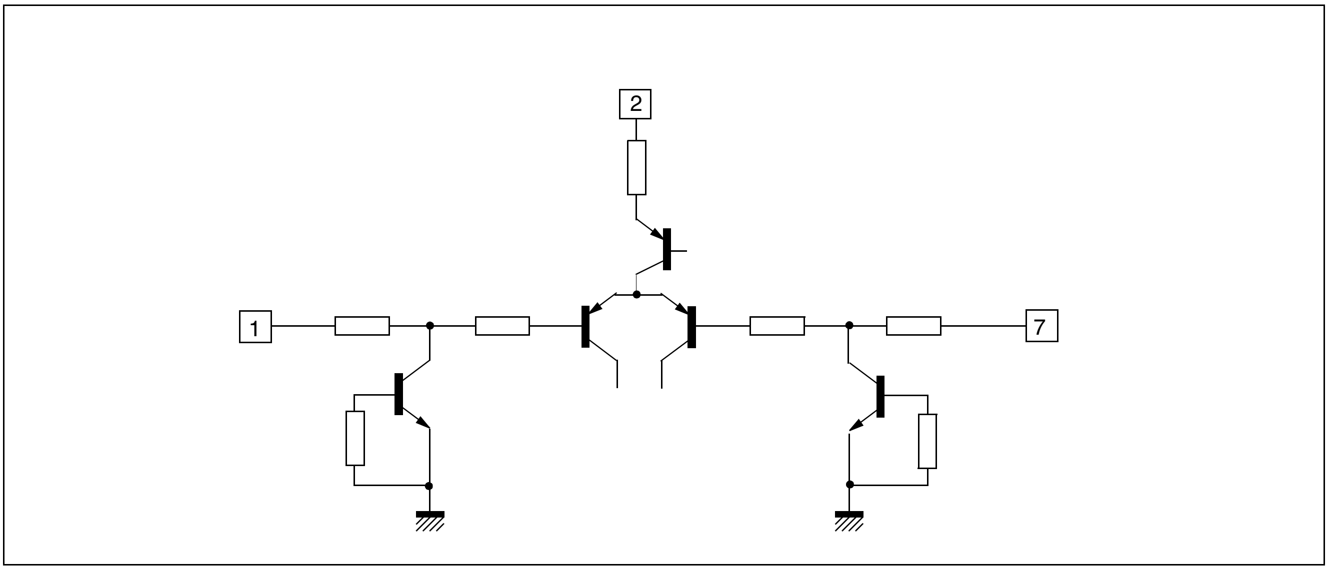
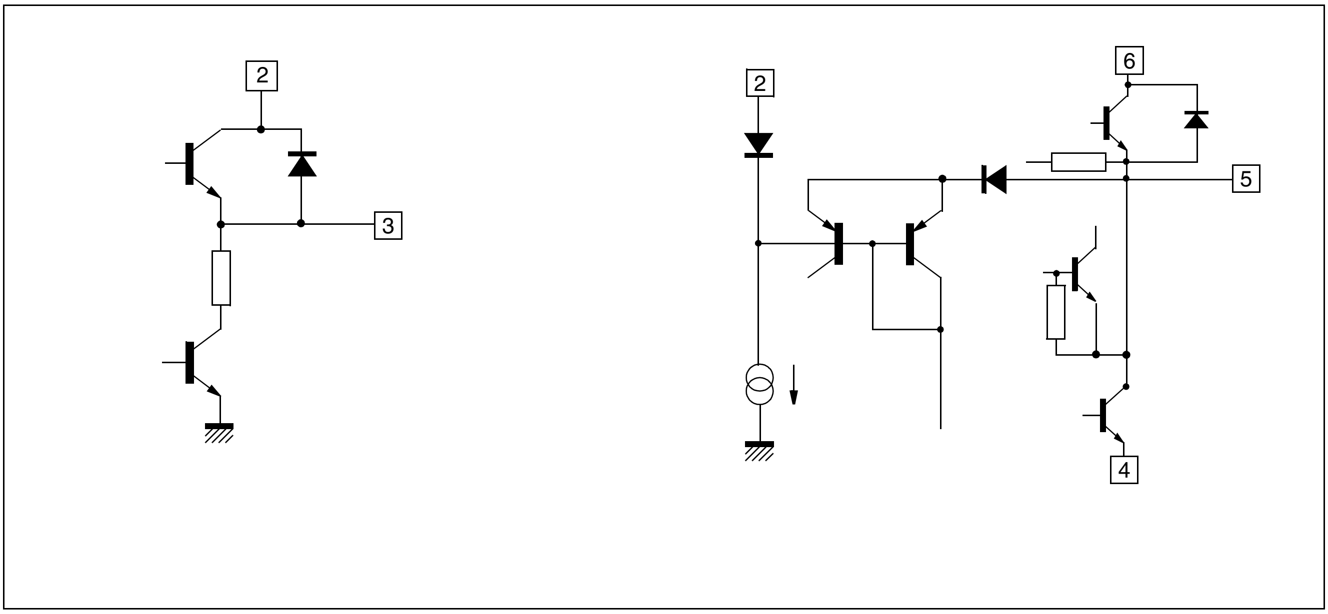


Figure 12: Pin 3 & Pins 5 and 6



7 Package Mechanical Data

Figure 13: 7-pin Heptawatt Package

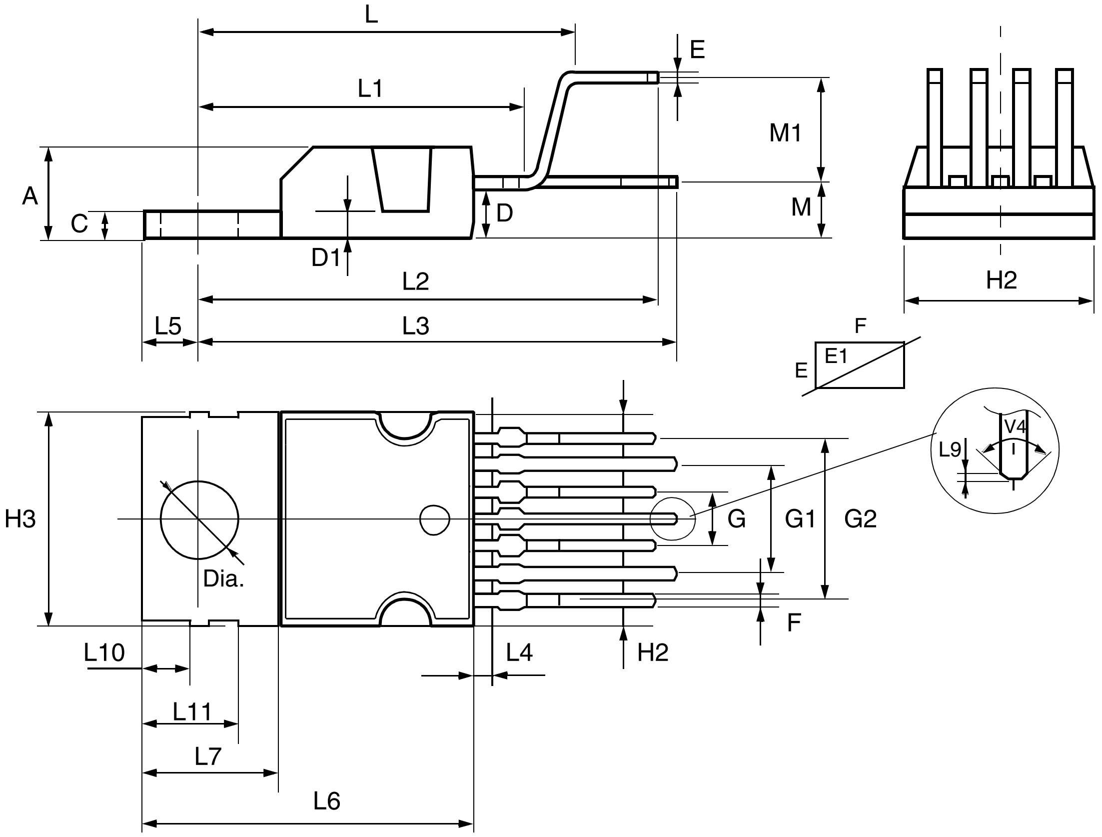


Table 1: Heptawatt Package

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.40		2.80	0.094		0.110
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.70		0.97	0.028		0.038
F	0.60		0.80	0.024		0.031
G	2.34	2.54	2.74	0.095	0.100	0.105
G1	4.88	5.08	5.28	0.193	0.200	0.205
G2	7.42	7.62	7.82	0.295	0.300	0.307
H2			10.40			0.409
H3	10.05		10.40	0.396		0.409
L	16.70	16.90	17.10	0.657	0.668	0.673

Table 1: Heptawatt Package (Continued)

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L1		14.92			0.587	
L2	21.24	21.54	21.84	0.386	0.848	0.860
L3	22.27	22.52	22.77	0.877	0.891	0.896
L4			1.29			0.051
L5	2.60	2.80	3.00	0.102	0.110	0.118
L6	15.10	15.50	15.80	0.594	0.610	0.622
L7	6.00	6.35	6.60	0.0236	0.250	0.260
L9		0.20			0.008	
L10	2.10		2.70	0.082		0.106
L11	4.30		4.80	0.169		0.190
M	2.55	2.80	3.05	0.100	0.110	0.120
M1	4.83	5.08	5.33	0.190	0.200	0.210
V4	40 (Typ.)					
Dia.	3.65		3.85	0.144		0.152

8 Revision History

Table 2: Summary of Modifications

Version	Date	Description
0.1	February 2005	First Issue