

# DATA SHEET

## **TDA4685**

Video processor with automatic  
cut-off control

Product specification  
Supersedes data of May 1993  
File under Integrated Circuits, IC02

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## Video processor with automatic cut-off control

## TDA4685

### FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or via I<sup>2</sup>C-bus; brightness and contrast control of both RGB inputs
- Saturation, contrast, brightness and white adjustment via I<sup>2</sup>C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2 or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control or clamped output selectable via I<sup>2</sup>C-bus
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I<sup>2</sup>C-bus
- Emitter-follower RGB output stages to drive the video output stages
- I<sup>2</sup>C-bus controlled DC output e.g. for hue-adjust of NTSC (multistandard) decoders.

### GENERAL DESCRIPTION

The TDA4685 is a monolithic integrated circuit with a luminance and a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e.g. with the multistandard decoder TDA4655 or TDA9160 plus delay line TDA4661 and the Picture Signal Improvement (PSI) IC, TDA467X, or from a feature module.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4685	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1



The required input signals are:

- Luminance and negative colour difference signals
- 2 or 3-level sandcastle pulse for internal timing pulse generation
- I<sup>2</sup>C-bus data and clock signals for microcontroller control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4685 includes full I<sup>2</sup>C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4685 is a simplified, pin compatible (except for pin 18) version of the TDA4680. The module address via I<sup>2</sup>C-bus can be used for both ICs; where a function is not included in the TDA4685 the I<sup>2</sup>C-bus command is not executed. The differences with the TDA4680 are:

- No automatic white level control; the white levels are determined directly by the I<sup>2</sup>C-bus data
- RGB reference levels for automatic cut-off control are not adjustable via I<sup>2</sup>C-bus
- Clamping delay is fixed
- Only contrast and brightness adjust for the RGB input signals
- The measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

The TDA4686 is like TDA4685 but intended for double line frequency application.

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## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage (pin 5)	7.2	8.0	8.8	V
$I_P$	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B – Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R – Y) input (peak-to-peak value)	–	1.05	–	V
$V_{14}$	3-level sandcastle pulse				
	H + V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	2-level sandcastle pulse				
	H + V	–	2.5	–	V
BK	–	4.5	–	V	
$V_{i(p-p)}$	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (peak-to-peak value)	–	0.7	–	V
$V_{o(b-w)}$	RGB outputs at pins 24, 22 and 20 (black-to-white value)	–	2.0	–	V
$T_{amb}$	operating ambient temperature	0	–	70	°C

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## BLOCK DIAGRAM

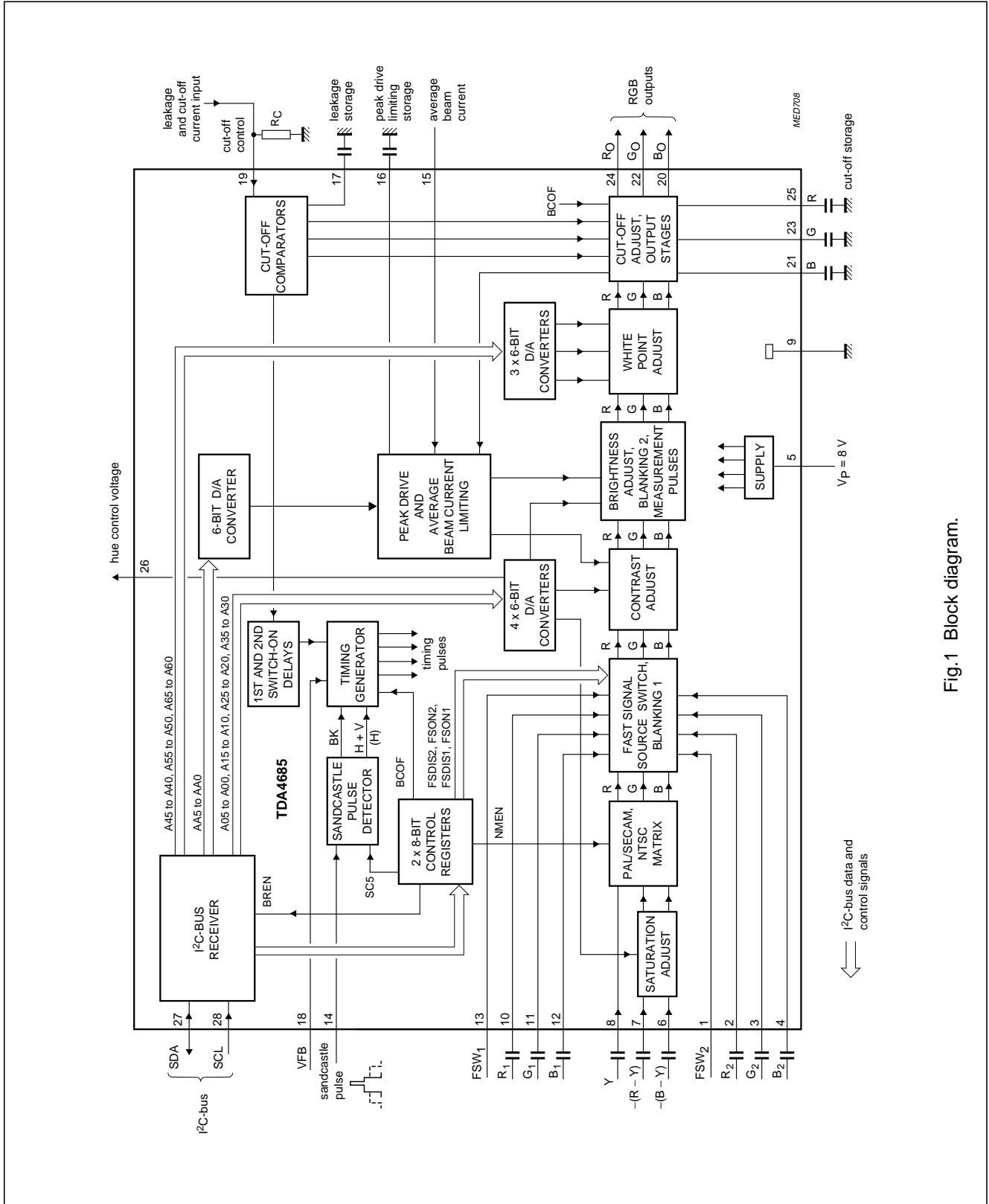


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
FSW <sub>2</sub>	1	fast switch 2 input
R <sub>2</sub>	2	red input 2
G <sub>2</sub>	3	green input 2
B <sub>2</sub>	4	blue input 2
V <sub>P</sub>	5	supply voltage
-(B - Y)	6	colour difference input -(B - Y)
-(R - Y)	7	colour difference input -(R - Y)
Y	8	luminance input
GND	9	ground
R <sub>1</sub>	10	red input 1
G <sub>1</sub>	11	green input 1
B <sub>1</sub>	12	blue input 1
FSW <sub>1</sub>	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C <sub>PDL</sub>	16	storage capacitor for peak drive limiting
C <sub>L</sub>	17	storage capacitor for leakage current
VFB	18	vertical flyback pulse input
CI	19	cut-off measurement input
B <sub>O</sub>	20	blue output
C <sub>B</sub>	21	blue cut-off storage capacitor
G <sub>O</sub>	22	green output
C <sub>G</sub>	23	green cut-off storage capacitor
R <sub>O</sub>	24	red output
C <sub>R</sub>	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I <sup>2</sup> C-bus serial data input; acknowledge output
SCL	28	I <sup>2</sup> C-bus serial clock input

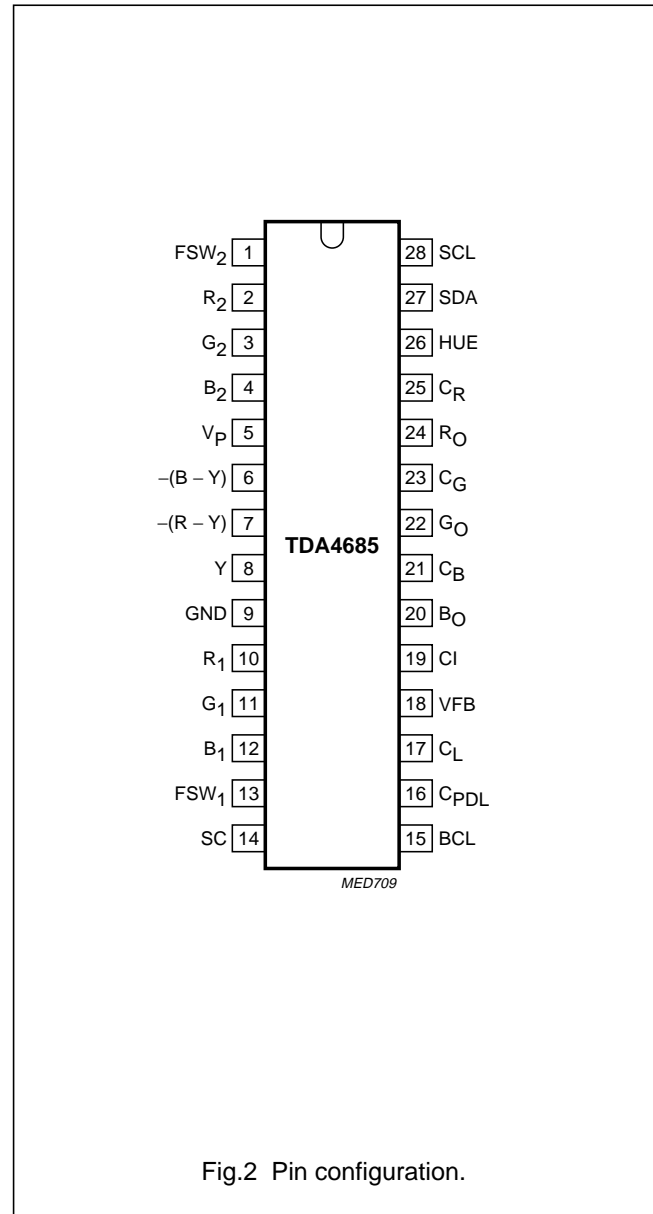


Fig.2 Pin configuration.

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### I<sup>2</sup>C-BUS PROTOCOL

#### Control

The I<sup>2</sup>C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- Brightness adjust
- Saturation adjust
- Contrast adjust
- DC output e.g. for hue control
- RGB gain adjust
- Peak drive limiting level adjust
- Selects either 3-level or 2-level (5 V) sandcastle pulse
- Enables cut-off control; enables output clamping
- Selects either PAL/SECAM or NTSC matrix
- Enables/disables synchronization of the execution of I<sup>2</sup>C-bus commands with the vertical blanking interval
- Enables Y/CD, RGB<sub>1</sub> or RGB<sub>2</sub> input.

#### I<sup>2</sup>C-bus transmitter and data transfer

##### I<sup>2</sup>C-BUS SPECIFICATION

The I<sup>2</sup>C-bus is a bidirectional, two-wire, serial data bus for intercommunication between ICs in an equipment.

The microcontroller transmits data to the I<sup>2</sup>C-bus receiver in the TDA4685 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a START bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a STOP bit.

Each transmission must start with a START bit and end with a STOP bit. The bus is busy after a START bit and is only free again after a STOP bit has been transmitted.

##### I<sup>2</sup>C-BUS RECEIVER (MICROCONTROLLER WRITE MODE)

Each transmission to the I<sup>2</sup>C-bus receiver consists of at least three bytes following the START bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module Address (MAD) byte, also called slave address byte. This includes the module address, 1000100 for the TDA4685. The TDA4685 is a slave receiver ( $R/\overline{W} = 0$ ), therefore the module address byte is 10001000 (88H; see also Fig.3).

The length of a data transmission is unrestricted, but the module address and the correct subaddress must be transmitted before the data byte(s). The order of data transmission is shown in Figs 4 and 5.

Without auto-increment (BREN = 0 or 1) the module address (MAD) byte is followed by a SubAddress (SAD) byte and one data byte only (see Fig.4).



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## AUTO-INCREMENT

The auto-increment format enables quick slave receiver initialization by one transmission, when the I<sup>2</sup>C-bus control bit BREN = 0 (see control register bits of Table 1).

If BREN = 1 auto-increment is not possible.

If the auto-increment format is selected, the MAD byte is followed by a SAD byte and by the data bytes of consecutive subaddresses (see Fig.5).

All subaddresses from 00H to 0FH are automatically incremented, the subaddress counter wraps round from 0FH to 00H. Reserved subaddresses 07H, 08H, 09H, 0BH, 0EH and 0FH are treated as legal but have no effect. Subaddresses outside the range 00H and 0FH are not acknowledged by the device.

Subaddresses are stored in the TDA4685 to address the following parameters and functions (see Table 1):

- Brightness adjust
- Saturation adjust
- Contrast adjust
- Hue control voltage
- RGB gain adjust
- Peak drive limiting adjust
- Control register functions.

The data bytes D7 to D0 (see Table 1) provide the data of the parameters and functions for video processing.

## CONTROL REGISTER 1

NMEN (NTSC Matrix Enable):

0 = PAL/SECAM matrix

1 = NTSC matrix.

BREN (Buffer Register Enable):

0 = new data is executed as soon as it is received

1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.

The I<sup>2</sup>C-bus receiver does not accept any new data until this data is transferred into the data registers.

SC5 (SandCastle 5 V):

0 = 3-level sandcastle pulse

1 = 2-level (5 V) sandcastle pulse.

## CONTROL REGISTER 2

FSON2 (Fast Switch 2 ON).

FSDIS2 (Fast Switch 2 Disable).

FSON1 (Fast Switch 1 ON).

FSDIS1 (Fast Switch 1 Disable).

The RGB input signals are selected by FSON2 and FSON1 or FSW<sub>2</sub> and FSW<sub>1</sub>:

- FSON2 has priority over FSON1
- FSW<sub>2</sub> has priority over FSW<sub>1</sub>
- FSDIS1 and FSDIS2 disable FSW<sub>1</sub> and FSW<sub>2</sub> (see Table 2).

BCOF (Black level Control Off):

0 = automatic cut-off control enabled

1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01H.



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**Table 1** Subaddress (SAD) and data bytes; note 1

FUNCTION	SAD (HEX)	MSB								LSB	
		D7	D6	D5	D4	D3	D2	D1	D0		
Brightness	00	0	0	A05	A04	A03	A02	A01	A00		
Saturation	01	0	0	A15	A14	A13	A12	A11	A10		
Contrast	02	0	0	A25	A24	A23	A22	A21	A20		
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30		
Red gain	04	0	0	A45	A44	A43	A42	A41	A40		
Green gain	05	0	0	A55	A54	A53	A52	A51	A50		
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60		
Reserved	07	0	0	X	X	X	X	X	X		
Reserved	08	0	0	X	X	X	X	X	X		
Reserved	09	0	0	X	X	X	X	X	X		
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0		
Reserved	0B	X	X	X	X	X	X	X	X		
Control register 1	0C	SC5	X	BREN	X	NMEN	X	X	X		
Control register 2	0D	X	X	X	BCOF	FSDIS2	FSON2	FSDIS1	FSON1		
Reserved	0E	X	X	X	X	X	X	X	X		
Reserved	0F	X	X	X	X	X	X	X	X		

**Note**

1. X = don't care, but for software compatibility with other or future video ICs it is recommended to set all X to logic 0.

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**Table 2** Signal input selection by the fast source switches; notes 1 to 4

I <sup>2</sup> C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW <sub>2</sub> (PIN 1)	FSW <sub>1</sub> (PIN 13)	RGB <sub>2</sub>	RGB <sub>1</sub>	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

**Notes**

1. H: logic HIGH implies that the voltage >0.9 V.
2. L: logic LOW implies that the voltage <0.4 V.
3. X = don't care.
4. ON indicates the selected input signal.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage (pin 5)	–	8.8	V
V <sub>i</sub>	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	–0.1	+V <sub>P</sub>	V
	input voltage (pins 15, 18 and 19)	–0.7	V <sub>P</sub> + 0.7	V
	input voltage (pins 27 and 28)	–0.1	+8.8	V
V <sub>14</sub>	sandcastle pulse voltage	–0.7	V <sub>P</sub> + 5.8	V
I <sub>av</sub>	average current (pins 20, 22 and 24)	–10	+4	mA
I <sub>M</sub>	peak current (pins 20, 22 and 24)	–20	+4	mA
I <sub>26</sub>	output current	–8	+0.6	mA
T <sub>stg</sub>	storage temperature	–20	+150	°C
T <sub>amb</sub>	operating ambient temperature	0	70	°C
P <sub>tot</sub>	total power dissipation	–	1.2	W

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**CHARACTERISTICS**

All voltages are measured in test circuit of Fig.9 with respect to GND (pin 9);  $V_P = 8.0$  V;  $T_{amb} = 25$  °C; nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20; nominal settings of brightness, contrast, saturation and white level control; without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply (pin 5)</b>						
$V_P$	supply voltage		7.2	8.0	8.8	V
$I_P$	supply current		–	60	–	mA
<b>Colour difference inputs [–(B – Y): pin 6; –(R – Y): pin 7]</b>						
$V_{6(p-p)}$	–(B – Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R – Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
$ I_{6,7} $	input current	during line scan	–	–	0.1	$\mu$ A
		at black level clamping	100	–	–	$\mu$ A
$R_{6,7}$	input resistance		10	–	–	M $\Omega$
<b>Luminance/sync (VBS; Y: pin 8)</b>						
$V_{i(p-p)}$	luminance input voltage at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
$V_{8(bias)}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
$ I_8 $	input current	during line scan	–	–	0.1	$\mu$ A
		at black level clamping	100	–	–	$\mu$ A
$R_8$	input resistance		10	–	–	M $\Omega$
<b>RGB input 1 (<math>R_1</math>: pin 10; <math>G_1</math>: pin 11; <math>B_1</math>: pin 12)</b>						
$V_{i(p-p)}$	input voltage at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12(bias)}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$ I_{10/11/12} $	input current	during line scan	–	–	0.1	$\mu$ A
		at black level clamping	100	–	–	$\mu$ A
$R_{10/11/12}$	input resistance		10	–	–	M $\Omega$
<b>RGB input 2 (<math>R_2</math>: pin 2, <math>G_2</math>: pin 3, <math>B_2</math>: pin 4)</b>						
$V_{i(p-p)}$	input voltage at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$ I_{2/3/4} $	input current	during line scan	–	–	0.1	$\mu$ A
		at black level clamping	100	–	–	$\mu$ A
$R_{2/3/4}$	input resistance		10	–	–	M $\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Fast signal switch FSW<sub>1</sub> (pin 13) to select Y, CD or R<sub>1</sub>, G<sub>1</sub>, B<sub>1</sub> inputs (control bits: see Table 2)</b>						
V <sub>13</sub>	voltage to select Y and CD		–	–	0.4	V
	voltage to select R <sub>1</sub> , G <sub>1</sub> , B <sub>1</sub>		0.9	–	5.0	V
R <sub>13</sub>	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
<b>Fast signal switch FSW<sub>2</sub> (pin 1) to select Y, CD/R<sub>1</sub>, G<sub>1</sub>, B<sub>1</sub> or R<sub>2</sub>, G<sub>2</sub>, B<sub>2</sub> inputs (control bits: see Table 2)</b>						
V <sub>1</sub>	voltage to select Y, CD/R <sub>1</sub> , G <sub>1</sub> , B <sub>1</sub>		–	–	0.4	V
	voltage to select R <sub>2</sub> , G <sub>2</sub> , B <sub>2</sub>		0.9	–	5.0	V
R <sub>1</sub>	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
<b>Saturation adjust [acts on –(R – Y) and –(B – Y) signals under I<sup>2</sup>C-bus control; subaddress 01H (bit resolution 1.5% of maximum saturation); data byte 3FH for maximum saturation, data byte 23H for nominal saturation and data byte 00H for minimum saturation]</b>						
d <sub>s</sub>	saturation below maximum	at 23H	–	5	–	dB
		at 00H; f = 100 kHz	–	50	–	dB
<b>Contrast adjust [acts on internal RGB signals under I<sup>2</sup>C-bus control; subaddress 02H (bit resolution 1.5% of maximum contrast); data byte 3FH for maximum contrast, data byte 22H for nominal contrast and data byte 00H for minimum contrast]</b>						
d <sub>c</sub>	contrast below maximum	at 22H	–	5	–	dB
		at 00H	–	22	–	dB
<b>Brightness adjust [acts on internal RGB signals under I<sup>2</sup>C-bus control; subaddress 00H (bit resolution 1.5% of maximum brightness); data byte 3FH for maximum brightness, data byte 26H for nominal brightness and data byte 00H for minimum brightness]</b>						
d <sub>br</sub>	black level shift of nominal signal amplitude referred to cut-off measurement level	at 3FH	–	30	–	%
		at 00H	–	–50	–	%
<b>White potentiometers [under I<sup>2</sup>C-bus control; subaddresses 04H (red), 05H (green) and 06H (blue); data byte 3FH for maximum gain; data byte 19H for nominal gain and data byte 00H for minimum gain]; note 3</b>						
ΔG <sub>v</sub>	relative to nominal gain					
	increase of gain	at 3FH	–	50	–	%
	decrease of gain	at 00H	–	50	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>RGB outputs (pins 24, 22 and 20; positive going output signals; peak drive limiter set = 3FH); note 4</b>						
$V_{o(b-w)}$	nominal output signals (black-to-white value)		–	2.0	–	V
	maximum output signals (black-to-white value)		3.0	–	–	V
$\Delta V_o$	spread between RGB output signals		–	–	10	%
$V_o$	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line equivalent to voltage during ultra-black	output clamping; BCOF = 1	2.3	2.5	2.7	V
$I_{int}$	internal current sources		–	5.0	–	mA
$R_o$	output resistance		–	20	–	$\Omega$
<b>Frequency response</b>						
$f_{res}$	frequency response of Y path (from pin 8 to pins 24, 22 and 20)	$f = 10$ MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	$f = 8$ MHz	–	–	3	dB
	frequency response of RGB <sub>1</sub> path (from pins 10 to 24, 11 to 22 and 12 to 20)	$f = 10$ MHz	–	–	3	dB
	frequency response of RGB <sub>2</sub> path (from pins 2 to 24, 3 to 22 and 4 to 20)	$f = 10$ MHz	–	–	3	dB
<b>Sandcastle pulse detector (pin 14)</b>						
CONTROL BIT SC5 = 0; 3-LEVEL; notes 5 and 6						
$V_{14}$	sandcastle pulse voltage					
	for horizontal and vertical blanking pulses		2.0	2.5	3.0	V
	for horizontal pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	$V_P + 5.8$	V
CONTROL BIT SC5 = 1; 2-LEVEL; notes 5 and 6						
$V_{14}$	sandcastle pulse voltage					
	for horizontal and vertical blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 5.8$	V
<b>GENERAL</b>						
$I_{14}$	output current	$V_{14} = 0$ V	–	–	–100	$\mu$ A
$t_d$	leading edge delay of the clamping pulse		–	1.5	–	$\mu$ s

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Vertical flyback (pin 18); note 6</b>						
V <sub>18</sub>	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open-circuit; note 7	–	5.0	–	V
I <sub>18</sub>	input current		–	–	5	μA
<b>Average beam current limiting (pin 15); note 8</b>						
V <sub>c(15)</sub>	contrast reduction starting voltage		–	4.0	–	V
ΔV <sub>c(15)</sub>	voltage difference for full contrast reduction		–	–2.0	–	V
V <sub>br(15)</sub>	brightness reduction starting voltage		–	2.5	–	V
ΔV <sub>br(15)</sub>	voltage difference for full brightness reduction		–	–1.6	–	V
<b>Peak drive limiting voltage [pin 16; internal peak drive limiting level (V<sub>pdl</sub>) acts on RGB outputs under I<sup>2</sup>C-bus control; subaddress 0AH]; note 9</b>						
V <sub>20,22,24</sub>	minimum RGB output voltages	at 00H	–	–	3.0	V
	maximum RGB output voltages	at 3FH	7.0	–	–	V
I <sub>16</sub>	charge current		–	–1	–	μA
	discharge current	during peak white	–	5	–	mA
V <sub>16</sub>	internal voltage limitation		4.5	–	–	V
V <sub>c(16)</sub>	contrast reduction starting voltage		–	4.0	–	V
ΔV <sub>c(16)</sub>	voltage difference for full contrast reduction		–	–2.0	–	V
V <sub>br(16)</sub>	brightness reduction starting voltage		–	2.5	–	V
ΔV <sub>br(16)</sub>	voltage difference for full brightness reduction		–	–1.6	–	V
<b>Automatic cut-off control (pin 19); notes 6 and 10 to 12; see Fig.7</b>						
V <sub>19</sub>	external voltage		–	–	V <sub>P</sub> – 1.4	V
I <sub>19</sub>	output current		–	–	–60	μA
	input current		150	–	–	μA
	additional input current	switch-on delay 1	–	0.5	–	mA
V <sub>24,22,20</sub>	monitor pulse amplitude (under I <sup>2</sup> C-bus control; subaddress 0AH)	switch-on delay 1; note 11	–	V <sub>pdl</sub> – 1.0	–	V
V <sub>19(th)</sub>	voltage threshold for picture tube cathode warming up	switch-on delay 1	–	4.5	–	V
V <sub>ref</sub>	internally controlled voltage	during leakage measurement period	–	2.7	–	V
ΔV <sub>19</sub>	difference between V <sub>MEAS</sub> (cut-off measurement voltage) and V <sub>ref</sub>		–	1.0	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Cut-off storage (pins 25, 23 and 21)</b>						
I <sub>21,23,25</sub>	charge and discharge currents	during cut-off measurement lines	–	0.3	–	mA
	input currents of storage inputs	outside measurement time	–	–	0.1	μA
<b>Storage of leakage information (pin 17)</b>						
I <sub>17</sub>	charge and discharge currents	during leakage measurement period	–	0.4	–	mA
	leakage current	outside measurement time	–	–	0.1	μA
V <sub>17</sub>	threshold voltage for reset to switch-on state		–	2.5	–	V
<b>Hue control (under I<sup>2</sup>C-bus control; subaddress 03H; data byte 3FH for maximum voltage; data byte 20H for nominal voltage and data byte 00H for minimum voltage); note 13</b>						
V <sub>26</sub>	output voltage	at 3FH	4.8	–	–	V
		at 20H	–	3.0	–	V
		at 00H	–	–	1.2	V
I <sub>int</sub>	current of the internal current source at pin 26		500	–	–	μA
<b>I<sup>2</sup>C-bus receiver clock SCL (pin 28)</b>						
f <sub>SCL</sub>	input frequency range		0	–	100	kHz
V <sub>IL</sub>	LOW-level input voltage		–	–	1.5	V
V <sub>IH</sub>	HIGH-level input voltage		3.0	–	6.0	V
I <sub>IL</sub>	LOW-level input current		–	–	–10	μA
I <sub>IH</sub>	HIGH-level input current		–	–	10	μA
t <sub>L</sub>	clock pulse LOW		4.7	–	–	μs
t <sub>H</sub>	clock pulse HIGH		4.0	–	–	μs
t <sub>r</sub>	rise time		–	–	1.0	μs
t <sub>f</sub>	fall time		–	–	0.3	μs
<b>I<sup>2</sup>C-bus receiver data input/output SDA (pin 27)</b>						
V <sub>IL</sub>	LOW-level input voltage		–	–	1.5	V
V <sub>IH</sub>	HIGH-level input voltage		3.0	–	6.0	V
I <sub>IL</sub>	LOW-level input current		–	–	–10	μA
I <sub>IH</sub>	HIGH-level input current		–	–	10	μA
I <sub>OL</sub>	LOW-level output current		3.0	–	–	mA
t <sub>r</sub>	rise time		–	–	1.0	μs
t <sub>f</sub>	fall time		–	–	0.3	μs
t <sub>SU;DAT</sub>	data set-up time		0.25	–	–	μs

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### Notes to the characteristics

1. The values of the  $-(B - Y)$  and  $-(R - Y)$  colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600  $\Omega$ .
3. The white potentiometers affect the amplitudes of the RGB output signals.
4. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
5. Sandcastle pulses are compared with internal threshold voltages independent of  $V_p$ . The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage.  
The internal threshold voltages (control bit SC5 = 0) are:
  - 1.5 V for horizontal and vertical blanking pulses
  - 3.5 V for horizontal pulses
  - 6.5 V for the burst key pulse.The internal threshold voltages (control bit SC5 = 1) are:
  - 1.5 V for horizontal and vertical blanking pulses
  - 3.5 V for the burst key pulse.
6. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.7a. If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.7b. In this case, the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
7. If no VFB pulse is applied, pin 18 can be left open-circuit or connected to  $V_p$ . If pin 18 is always LOW neither automatic cut-off control nor output clamping can happen.
8. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
9. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I<sup>2</sup>C-bus under subaddress 0AH. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
10. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Figs 6 and 7).
11. During picture cathode warming up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilizes, RGB output blanking is removed.
12. Range of cut-off measurement level at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
13. The hue control output at pin 26 is an emitter follower with current source.



## Video processor with automatic cut-off control

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**Table 3** Demodulator axes and amplification factors

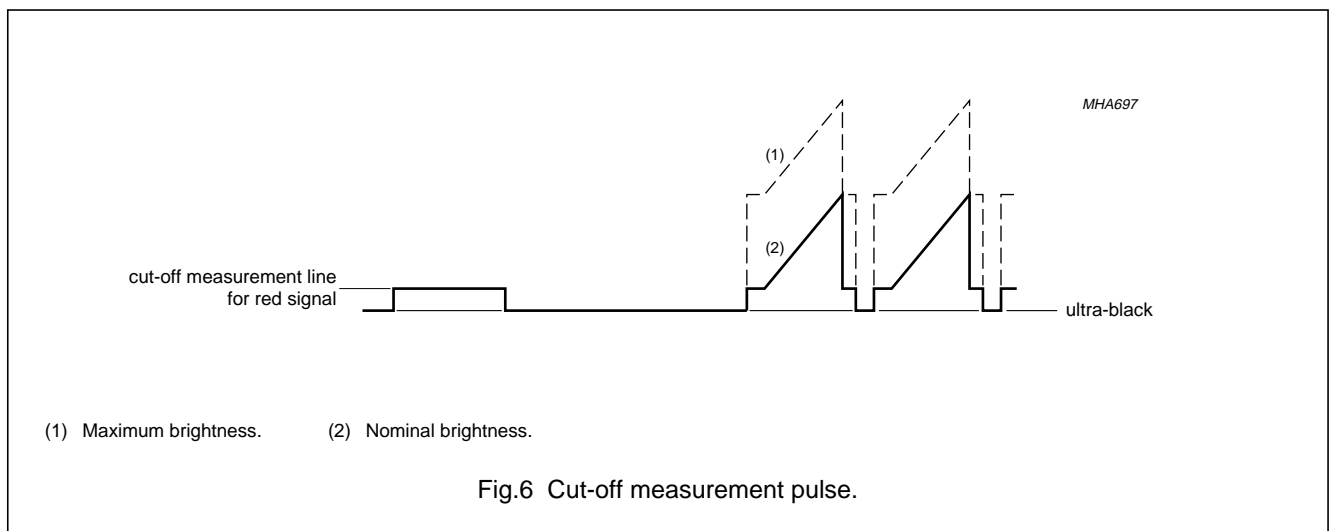
PARAMETER	NTSC	PAL
(B - Y)* demodulator axis	0°	0°
(R - Y)* demodulator axis	115°	90°
(R - Y)* amplification factor	1.97	1.14
(B - Y)* amplification factor	2.03	2.03

**Table 4** PAL/SECAM and NTSC matrix; note 1

MATRIX	NMEN
PAL/SECAM	0
NTSC	1

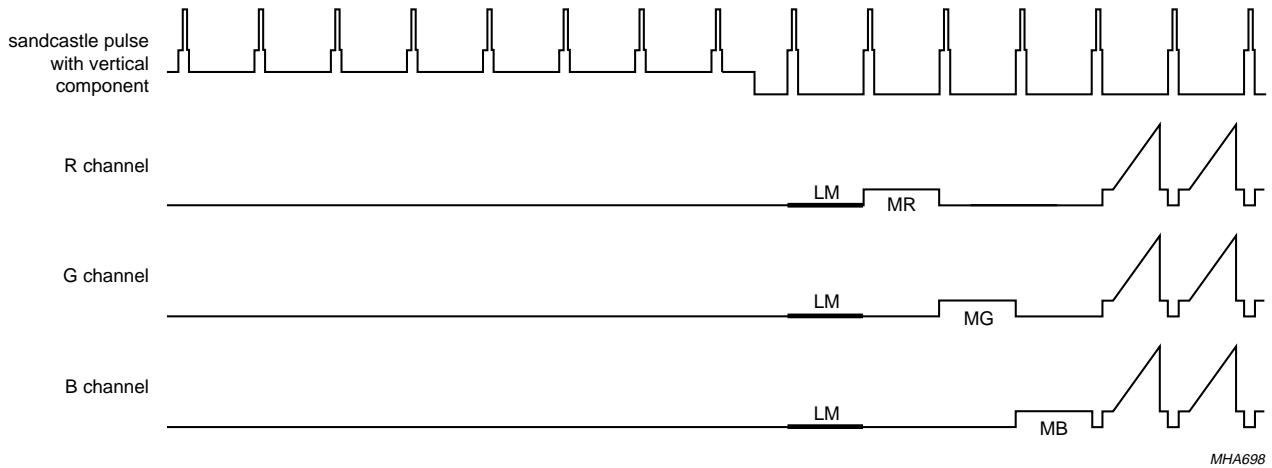
**Note**

- PAL/SECAM signals are matrixed by the equation:  $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$   
 NTSC signals are matrixed by the equations (hue phase shift of -5 degrees):  
 $V_{R-Y^*} = 1.57V_{R-Y} - 0.41V_{B-Y}$ ;  $V_{G-Y^*} = -0.43V_{R-Y} - 0.11V_{B-Y}$ ;  $V_{B-Y^*} = V_{B-Y}$   
 In the matrix equations:  $V_{R-Y}$  and  $V_{B-Y}$  are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.  $V_{G-Y^*}$ ,  $V_{R-Y^*}$  and  $V_{B-Y^*}$  are the NTSC modified colour difference signals; this is equivalent to the demodulator axes and amplification factors shown in Table 3.  $V_{G-Y^*} = -0.27V_{R-Y^*} - 0.22V_{B-Y^*}$ .



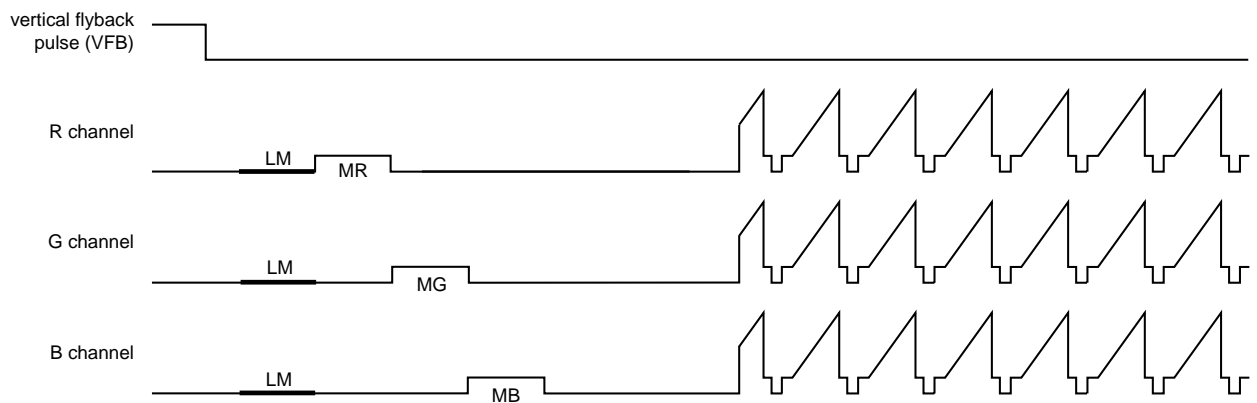
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MHA698

a. Timing controlled by sandcastle pulse.



MHA699

b. Timing controlled by additional vertical flyback pulse (VFB).

LM = leakage current measurement time.  
 MR, MG, MB = R, G, B cut-off measurement pulses.

Fig.7 Leakage and cut-off current measurement timing diagram.

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INTERNAL PIN CONFIGURATION

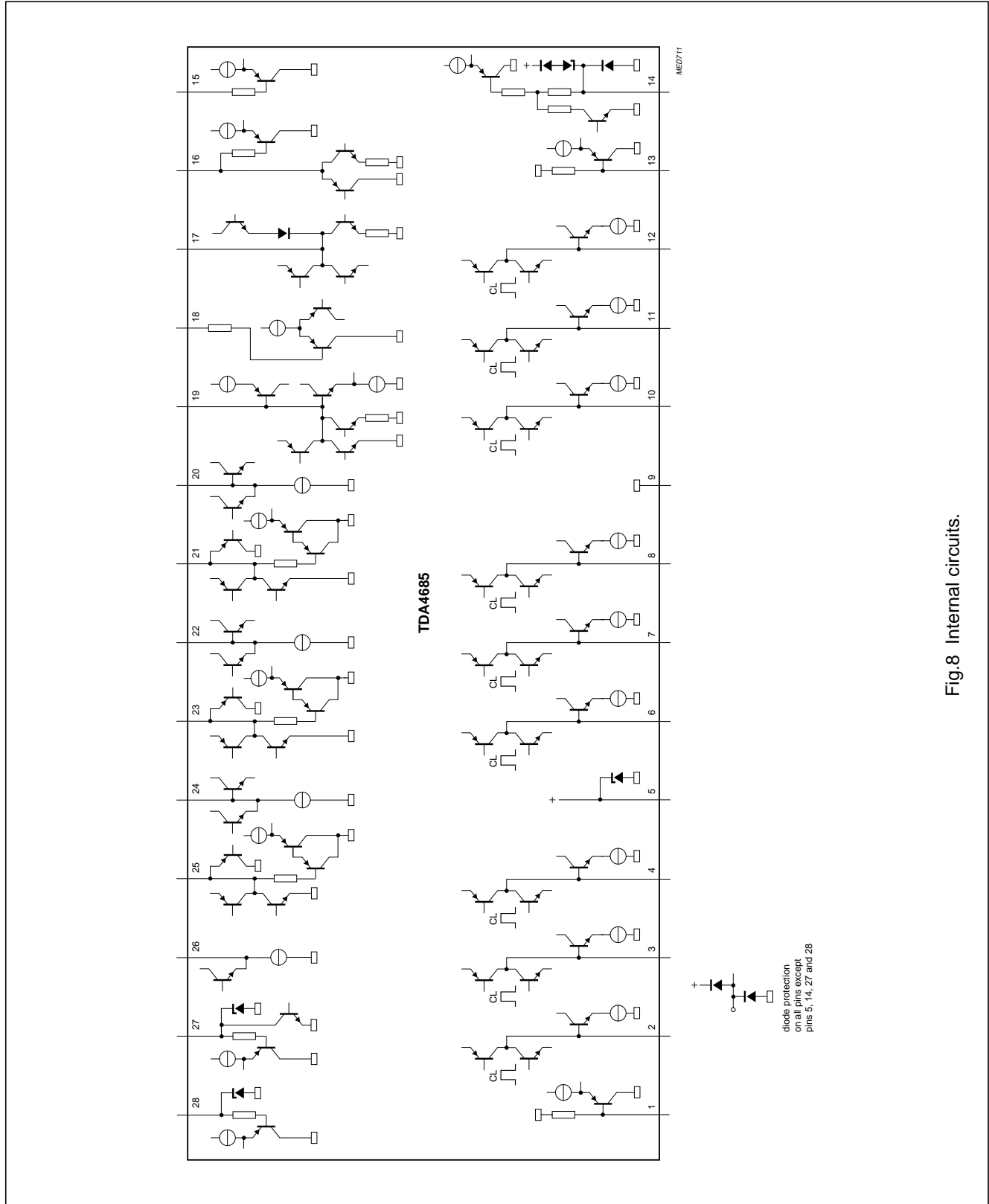


Fig.8 Internal circuits.



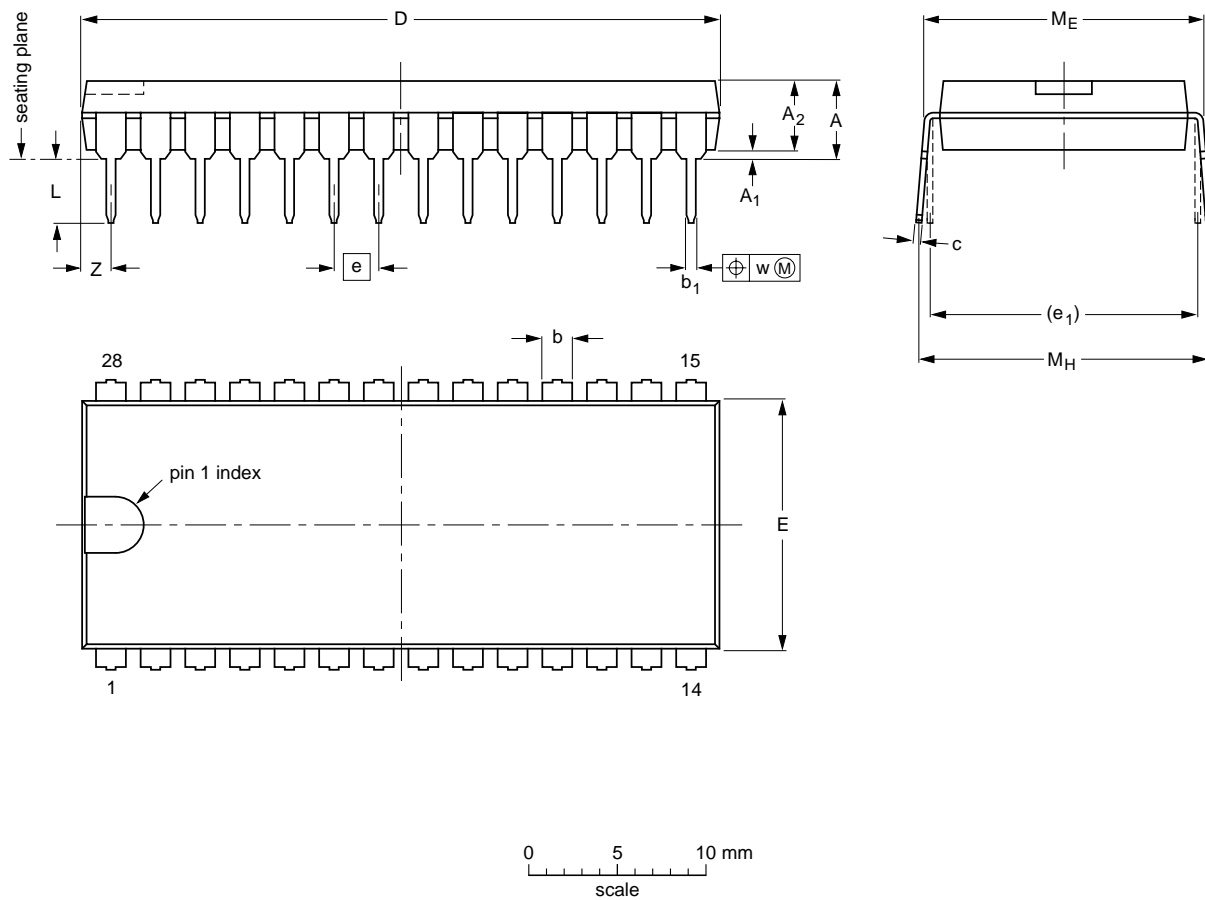
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PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				92-11-17 95-01-14

## Video processor with automatic cut-off control

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**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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