SIEMENS

Satellite-Video IC

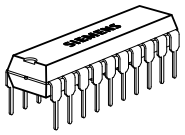
TDA 6151-5
TDA 6151-5X

Preliminary Data

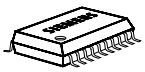
Bipolar IC

Features

- Adjustable gain for different FM deviations
- Video buffer and special baseband output for the sound processor SDA 6102-5X are available
- Clamping circuit for elimination of "Energy Dispersal" signal
- Built-in video switch for external applied video signal
- Application in satellite receiving systems.



P-DIP-20-1



P-DSO-20-1

Type	Ordering Code	Package
TDA 6151-5	Q67000-A5175	P-DIP-20-1
TDA 6151-5X	Q67000-A5074	P-DSO-20-1 (SMD)

The video circuit for a satellite application consists of a voltage controlled AGC-amplifier, driver for two external de-emphasis networks, followed by a three-stage switch. An additional baseband output is available via a driver. The output signal of the video switch is applied to a video clamping circuit, this clamping circuit removes the energy dispersal signal from the video signal. The clamped signal is applied via a video switch to the SCART-output.

Circuit Description

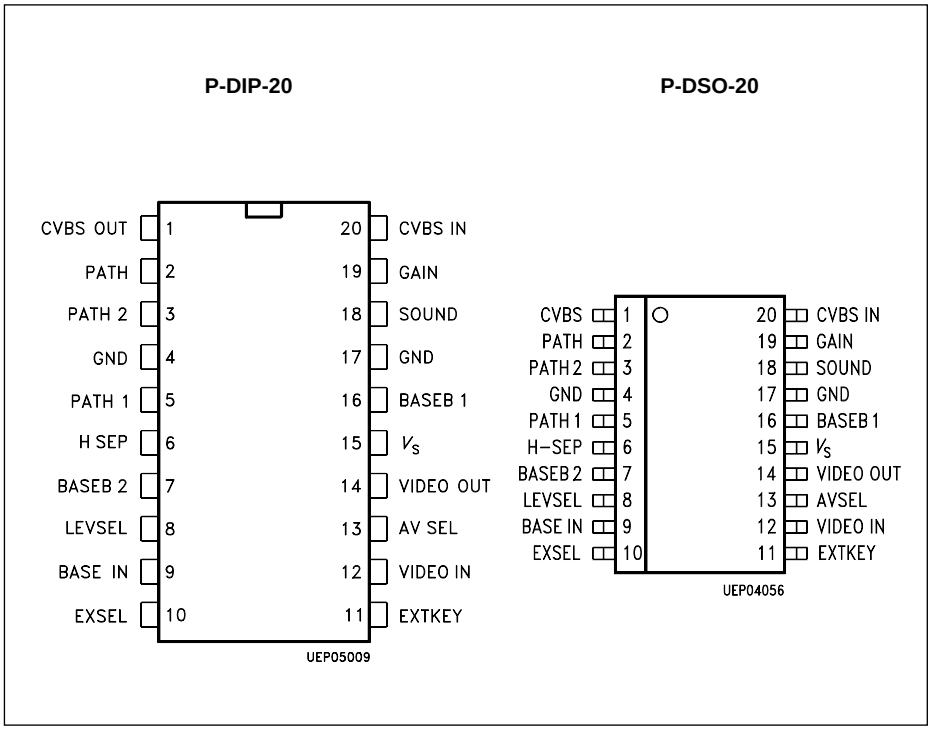
The demodulated FM-satellite video signal is fed via a buffer amplifier to a gain controlled amplifier. The gain control is done using an external applied DC-voltage. The output signal of this amplifier is used to drive three separate signal pathes. First of all the baseband is fed via a high pass filter with a cut off frequency of approx. 4 MHz to the input of a SAT-TV-sound processor, e.g. TDA 6160 X. A second output with a buffer amplifier is used to drive two external de-emphasis networks. After passing through the de-emphasis networks the baseband signals are fed into two inputs of the de-

emphasis selector switch. The third output of the gain controlled amplifier has a direct connection to the de-emphasis selector switch. This allows the selection of the sufficient frequency response of the de-emphasis network or a linear frequency response by passing the de-emphasis networks.

The output signal of the de-emphasis selector switch is fed separately via two driver amplifiers to the baseband 1 output and to the baseband 2 output. This baseband 2 output is fed via an external low pass filter to the input of the energy dispersal clamping circuit. This circuit removes the energy dispersal signal from the baseband signal. The clamping circuit can be operated with an internally generated clamping signal or a clamp pulse applied to the IC from an external source.

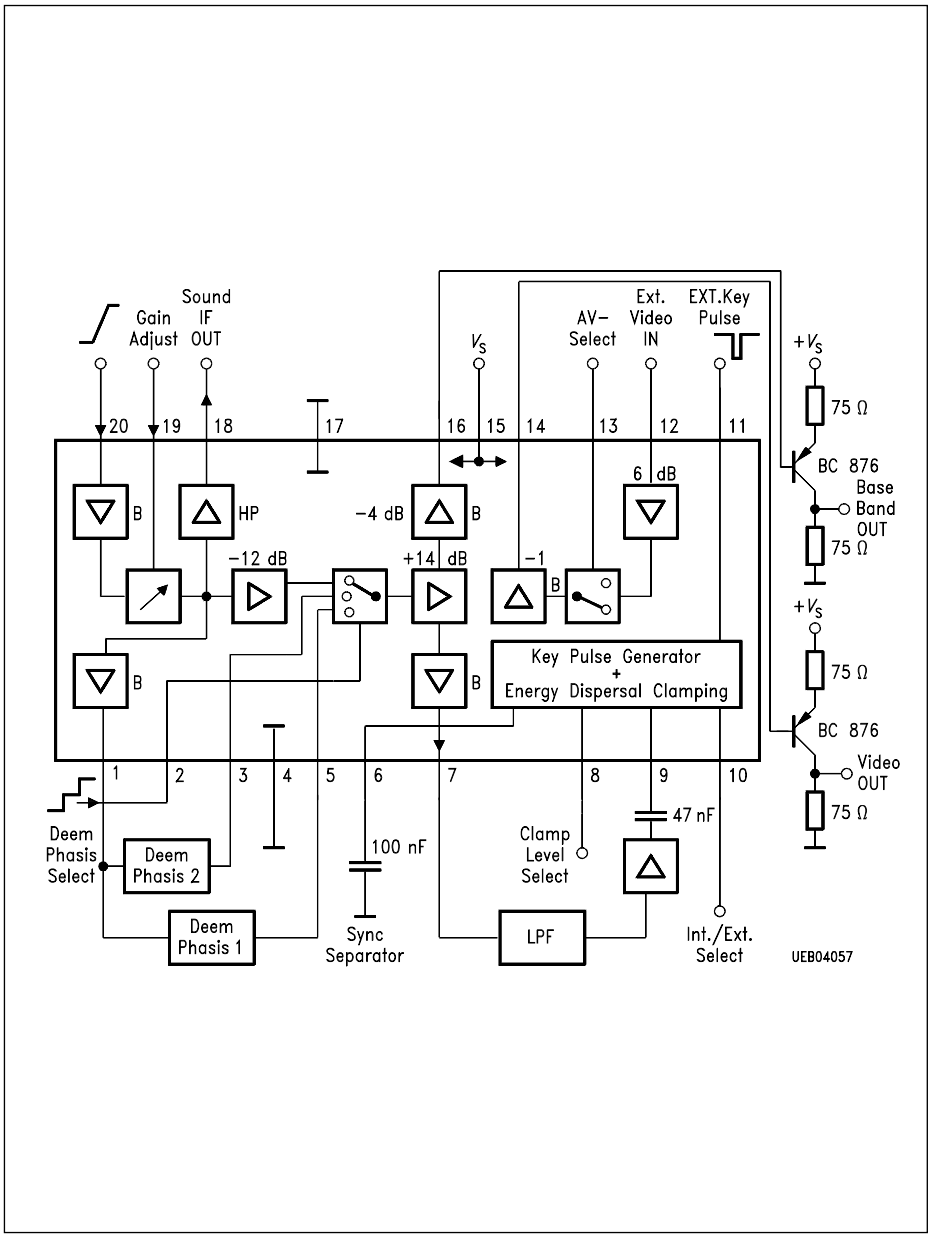
The internal generated clamping pulse can only be used if the incoming baseband signal is a standard CVBS-signal. The clamping pulse is then located in the H-sync pulse period. The impulse width is approx. 2 µs. The external clamping pulse must be active low. The timing of the pulse is not critical. The clamping level used in conjunction with the video signal can be selected according to the operation mode (CVBS- or MAC-mode). The clamping level differs by 1 V. The baseband output (pin 16) and CVBS-output (pin 14) require 75 Ω line drivers implemented as internal drivers followed by a PNP-emitter follower.

Pin Configuration
(top view)



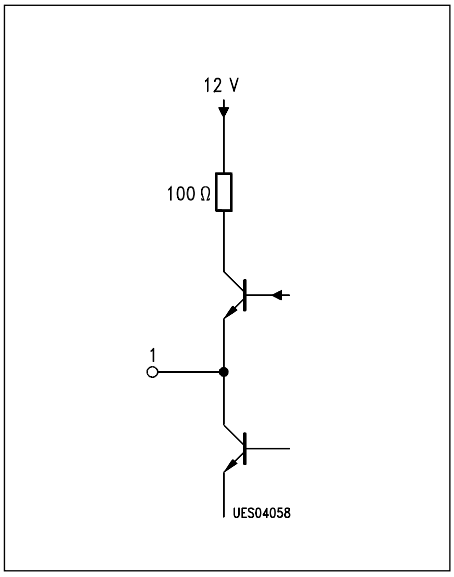
Pin Definitions and Functions

Pin No.	Symbol	Function
1	CVBS	CVBS-output (controlled)
2	PATH	De-emphasis select
3	PATH 2	De-emphasis 2 input
4	GND	Ground
5	PATH 1	De-emphasis 1 input
6	H-SEP	Sync separator
7	BASEB 2	Baseband output 2
8	LEVSEL	Clamping level select
9	BASE IN	Baseband input
10	EXSEL	Int./ext. clamping select
11	EXTKEY	Ext. key pulse input
12	VIDEO IN	Ext. video input
13	AVSEL	AV select
14	VIDEO OUT	Video output
15	V_S	Supply voltage
16	BASE B1	Baseband output 1
17	GND	Ground
18	SOUND	Sound output
19	GAIN	GAIN adjust
20	CVBS IN	CVBS-input

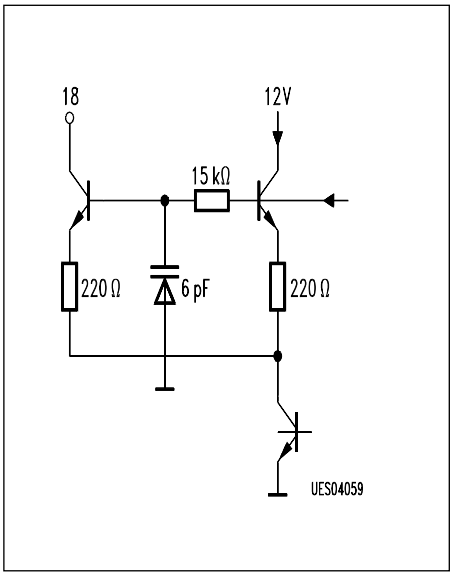


Block Diagram

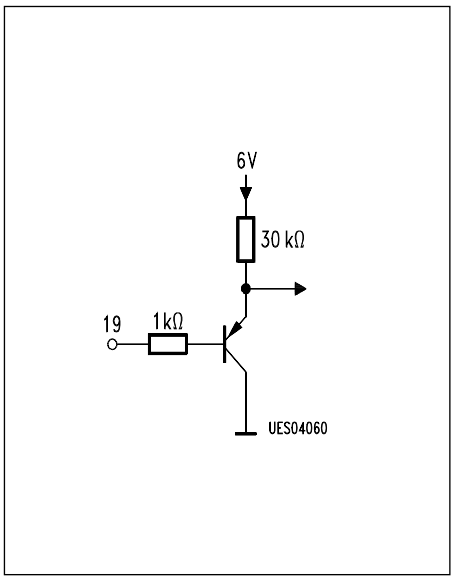
Pin Functions



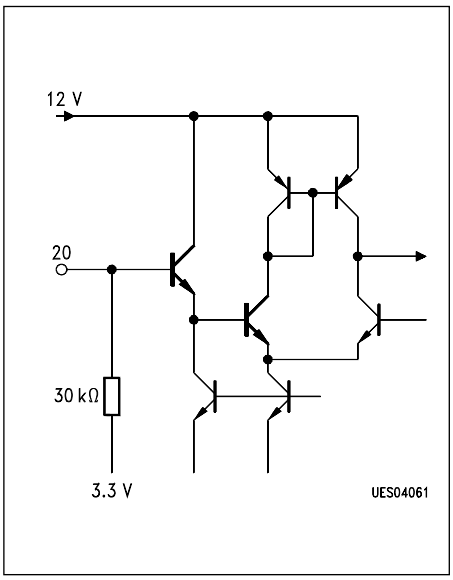
CVBS (Pin 1)



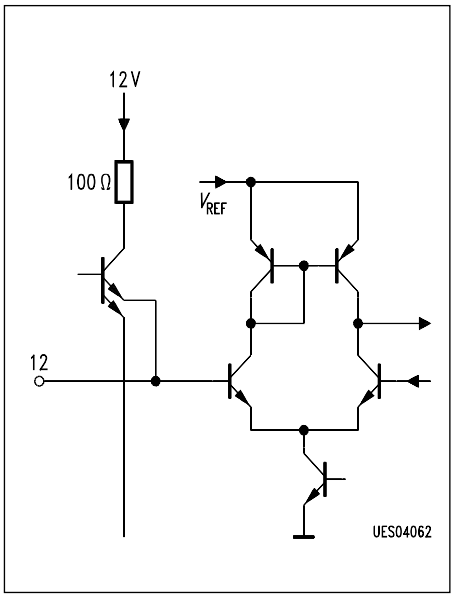
SOUND (Pin 18)



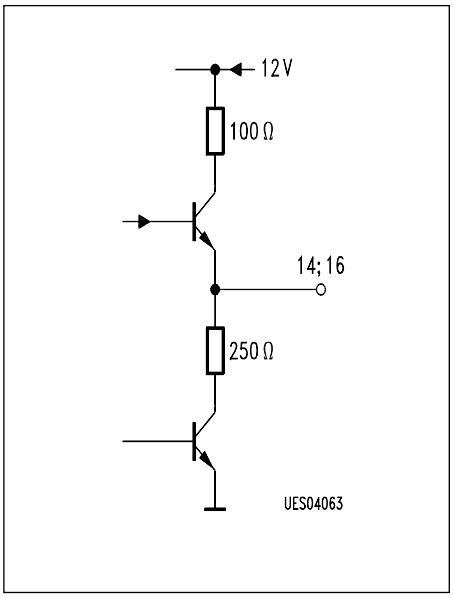
GAIN (Pin 19)



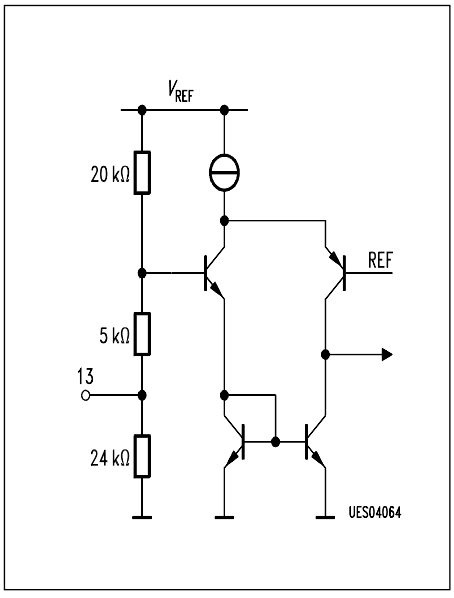
CVBS IN (Pin 20)



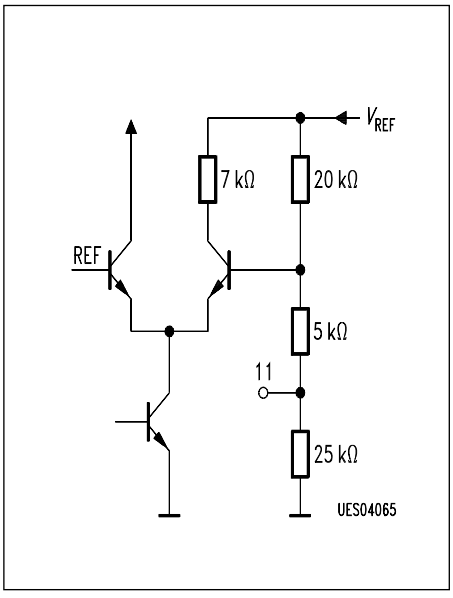
VIDEO IN (Pin 12)



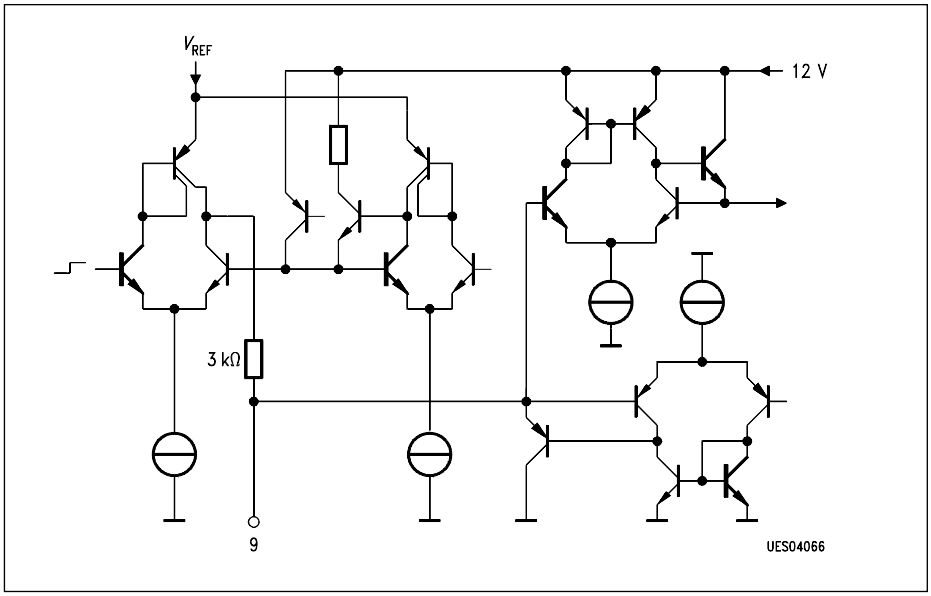
VIDEO OUT, BASEB1 (Pin 14, 16)



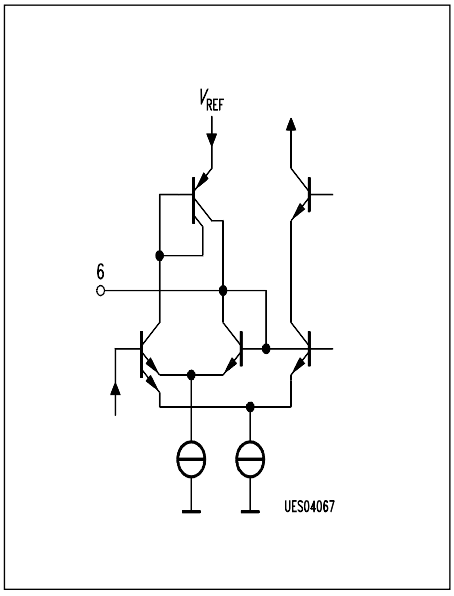
AVSEL (Pin 13)



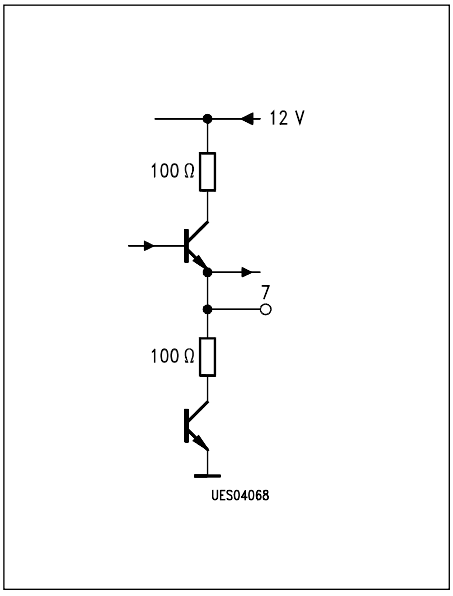
EXTKEY (Pin 11)



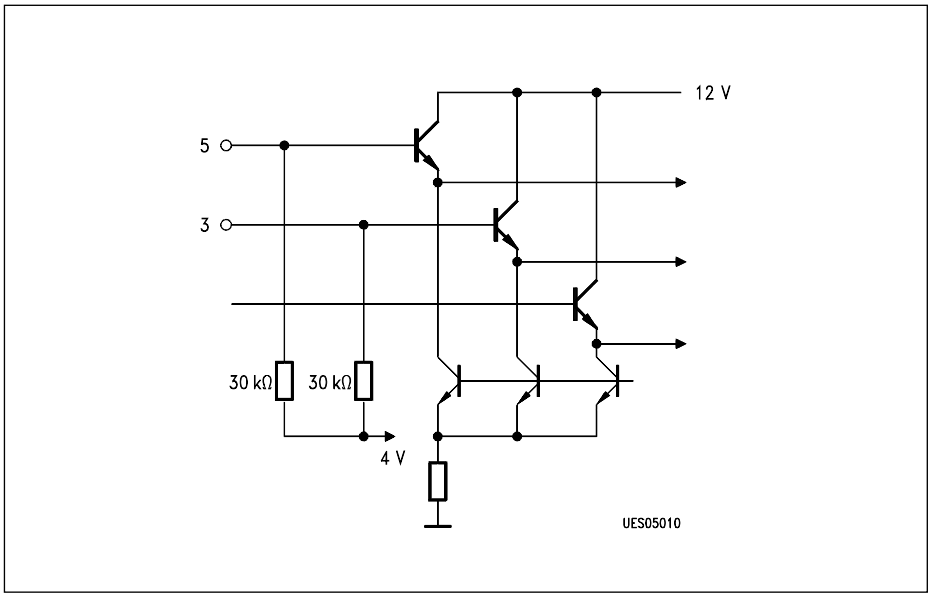
BASE IN (Pin 9)



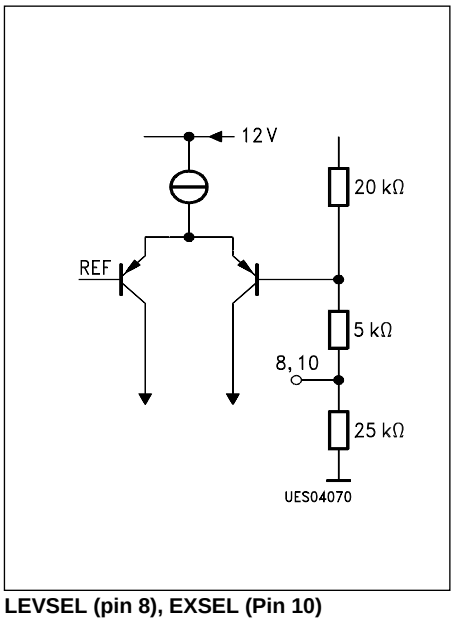
H-SEP (Pin 6)



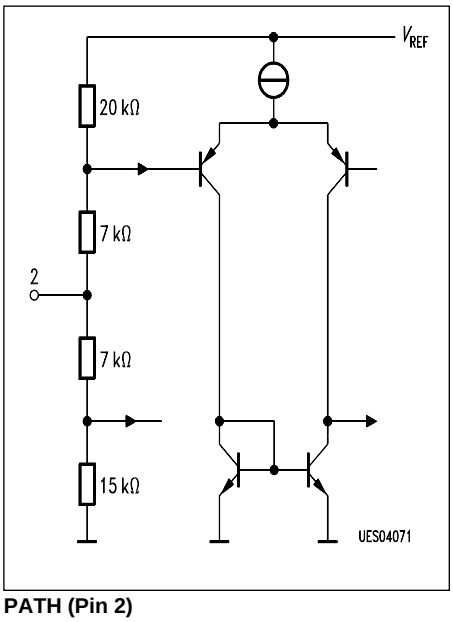
BASEB2 (Pin 7)



PATH1/PATH2 (Pin 5, 3)



LEVSEL (pin 8), EXSEL (Pin 10)



PATH (Pin 2)

Absolute Maximum Ratings

T_A = 0 to 70 °C

All voltage are referred to ground, unless stated otherwise. All currents are designated by the source and sink principle, i.e. if the device pin has to be regarded as a sink (the current flows in the started pin to the internal ground), it has a negative prefix; if the device pin is the source on the other hand (the current flows from V_S across the stated pin), it has a positive prefix.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{15}	0	15	V
Buffer output current (de-emphasis)	I_1	– 3	5	mA
Voltage on sound IF output	V_{18}		16	V
Video buffer output currents	$I_{14, 16}$	– 3	5	mA
Setting voltages for gain adjust	$V_{2, 19}$	0	6	V
Switching voltages for video switch	V_{13}	0	6	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance system air	$R_{th\ SA}$		65/77*	K/W
Operating Range				
Supply voltage	V_{15}	10.8	13.2	V
Input frequency range	f_{20}	10 Hz**	15	MHz
Frequency range of sound IF output coupling stage	f_{18}	4	10	MHz
3 -dB band width of baseband output	B_{16}	10		MHz
Ambient temperature in operation	T_A	0	70	°C

* SMD Package

** Depending on the used coupling capacitors

DC-Characteristics
T_A = 25 °C; V_S = 12 V

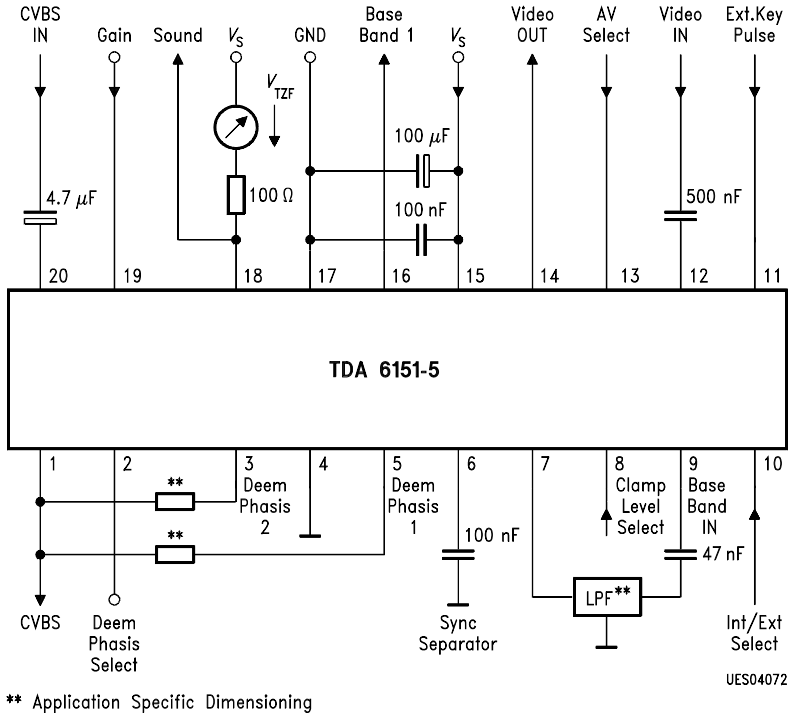
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{15}	26	38	50	mA	
Input voltage	V_{20}	3	3.3	3.6	V	
Input current	I_{20}	3.5	5	6.5	µA	ΔV_{20} = 0,15 V
Output voltage of de-emphasis buffer	V_1	3.75	4.15	4.55	V	V_{20} = 0 V_{PP}
Quiescent current of de-emphasis output	I_1	– 2.5	– 3.7	– 4.8	mA	$V_1 = V_1$ + 350 mV
Resistive load of de-emphasis output	$R_{1/4}$	1.5			kΩ	
Sound IF output current	I_{18}	350	500	650	µA	V_{18} = 12 V
Input current on de-emphasis inputs	$I_{3,5}$		± 5		µA	$\Delta V_{3,5}$ = ± 0.15 V
Output voltages of baseband buffer	V_{16}	V_S – 3.9	V_S – 3.25	V_S – 2.6	V	V_{19} = 5 V, V_{20} = 0 V_{PP}, $V_{3,5} = V_1$
Quiescent current of baseband buffer	I_{16}	– 2.5	– 3.2	– 4.2	mA	$V_{16} = V_{16}$ + 350 mV
Output voltage at low pass output	V_7	3.35	4.15	4.95	V	V_{19} = 0 V, V_{20} = 0 V_{PP}, $V_{3,5} = V_1$
Quiescent current at low pass output	I_7	– 2.3	– 3.0	– 3.9	mA	$V_7 = V_7$ + 350 mV
Resistive load of low pass output	$R_{7/4}$	1.5			kΩ	
Input current of clamping circuit	I_9	3.5	6	10	µA	V_9 = 3 V, 5 V > V_8 > 2 V
Output voltage of video buffer	V_{14}	V_S – 3.9	V_S – 3.2	V_S – 2.5	V	5 V > V_{13} > 2 V, V_{12} = 0 V_{PP}
Quiescent current of video buffer	I_{14}	– 2.0	– 2.7	– 3.4	mA	V_{14} = 12 V
Input current ext. CVBS-input	I_{12}	0.13	0.4	1	µA	
Setting voltage for deviation	V_{19}	0		5	V	
Gain Gain (see diagram)	$V_{1/20}$ $V_{1/20}$	17 0	21 1.5	25 3	dB dB	V_{19} = 0 V, V_{19} = 5 V

DC-Characteristics (cont'd)

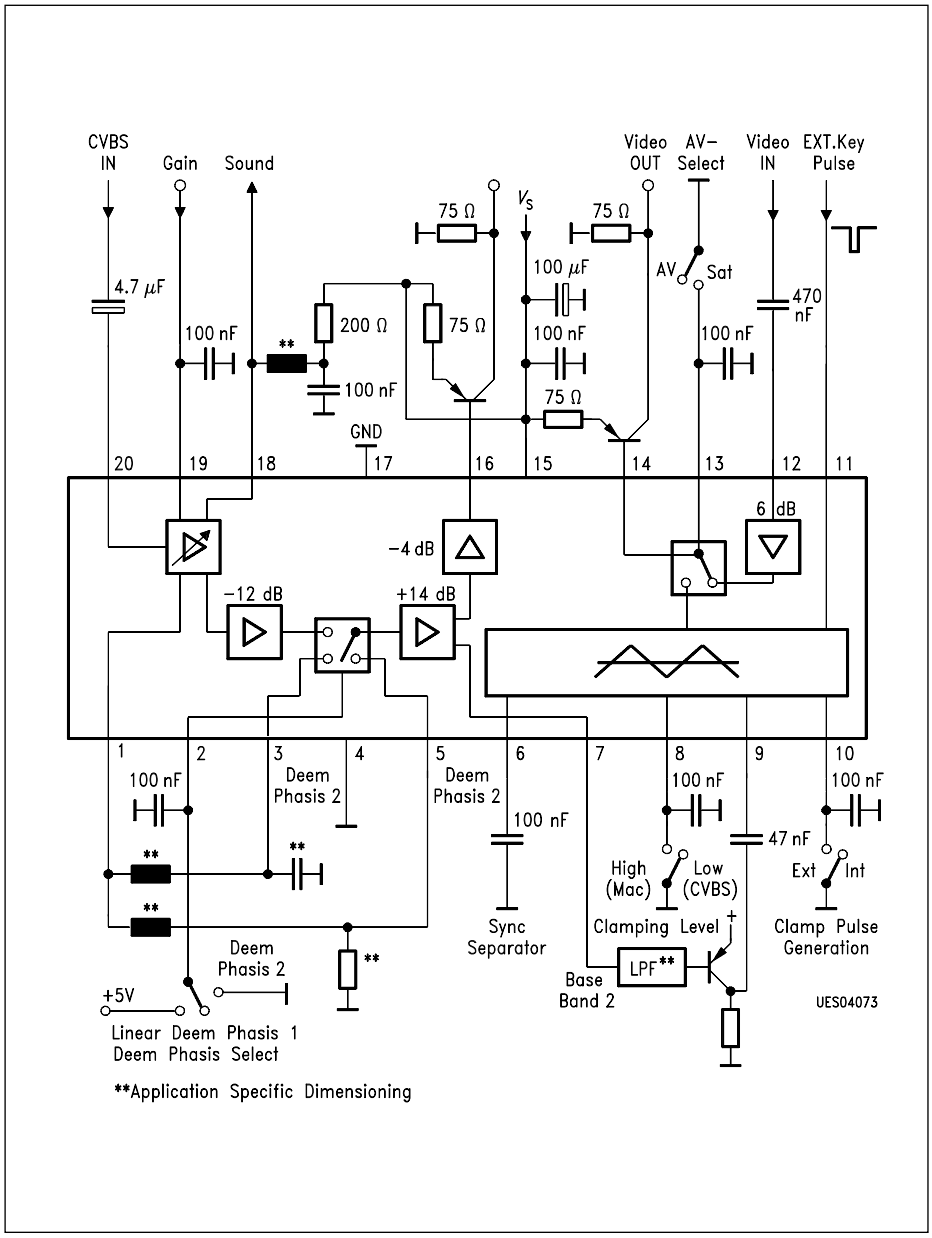
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching level for de-emphasis	V_2					
L = de-emphasis 2		0		1	V	
M (or open) = de-emphasis 1		2.3	2.8	3.3	V	
H = linear		4.0		5	V	
Switching level for video switch	V_{13}					
L = RF-mode		0		1	V	
H (or open) = external		2		5	V	
Input current of the switches	$I_{2,13,8,10}$					
H		– 300	– 200	– 100	µA	
L		100	200	330	µA	
Switching level for setting the clamping level	V_8					
L = high level (Mac operation)		0		1	V	
H (or open) = low clamping level (CVBS operation)		2		5	V	
Switching level for setting the clamping mode	V_{10}					
L = external clamping (Mac operation)		0		1	V	
H (or open) = internal (CVBS-operation)		2		5	V	

AC-Characteristics
T_A = 25 °C; V_S = 12 V

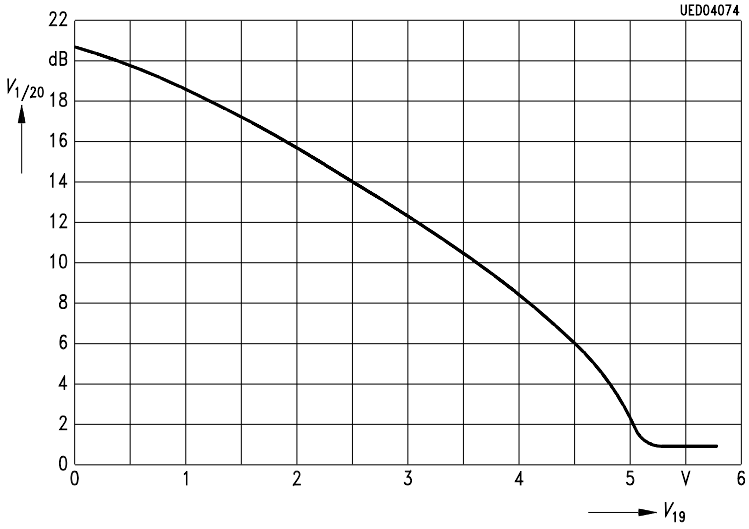
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input voltage range	V_{20}	0.2		1	V_{PP}	
Input impedance	R_{20}	22	31	42	kΩ	
Sound IF-output frequency range (– 3 dB)	f_{18}		4		MHz	V_{20} = 1 V, $R_{18/15}$ = 200 Ω
Sound IF-output upper frequency limit (– 3 dB)	f_{18}		10		MHz	V_{20} = 1 V, $R_{18/15}$ = 200 Ω
Output voltage	V_{18}		30		mV_{PP}	TT_{20} = 130 mV_{PP} $R_{18/15}$ = 200 Ω
Gain 10 MHz 4 MHz 400 kHz	$G_{1/18}$		– 17 – 26 – 80		dB dB dB	$R_{18/15}$ = 200 Ω
Output voltage of de-emphasis buffer	V_1		2		V_{PP}	V_{20} = 1 V_{PP} V_{19} = 4,4 V
Output voltage of baseband buffer	V_{16}		2		V_{PP}	V_7 = 3 V_{PP}
Output voltage	V_7		3		V_{PP}	V_1 = 2.4 V_{PP}
Gain	$V_{7/3;5}$		14		dB	
Gain	$V_{16/3;5}$		10		dB	
Gain	$V_{7/1}$		2		dB	linear path (de-emphasis)
Suppression of the energy dispersal signal	EDR	46			dB	V_{20} = 1 V_{PP} measured at the synch pulse
Output voltage video buffer	V_{14}		2		V_{PP}	V_9 = 2 V_{PP}
Gain AV-input video buffer	$V_{14/12}$		2			V_{12} = 1 V_{PP}
Gain (clamping input video buffer)	$V_{14/9}$		0		dB	V_9 = 1 V_{PP} (without triangular signal)
External clamping pulse L = active H (or open) = inactive			 0 2	 1 5	 V V	



Test Circuit



Application Circuit


UED04074
22
dB
$V_{1/20}$
18
16
14
12
10
8
6
4
2
0
0
1
2
3
4
5
V
6
V_{19}