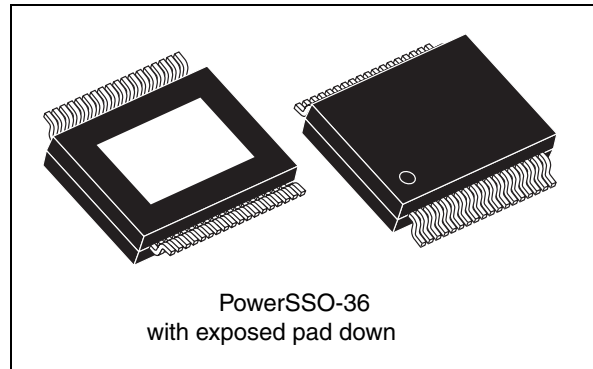


## 25-watt + 25-watt dual BTL class-D audio amplifier

### Features

- 25 W + 25 W continuous output power at THD = 10% with  $V_{CC} = 20\text{ V}$  and  $R_L = 8\ \Omega$
- Wide-range single-supply operation (8 - 26 V)
- High efficiency ( $\eta = 90\%$ )
- Four selectable, fixed gain settings of nominally 21.6 dB, 27.6 dB, 31.1 dB and 33.6 dB
- Differential inputs minimize common-mode noise
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable
- ECOPACK<sup>®</sup>, environmentally-friendly package



### Description

The TDA7492P is a dual BTL class-D audio amplifier with single power supply, designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-down (EPD) package no heatsink is required.

**Table 1. Device summary**

Order code	Operating temp. range	Package	Packaging
TDA7492P	-40 to 85 °C	PowerSSO-36 EPD	Tube
TDA7492P13TR	-40 to 85 °C	PowerSSO-36 EPD	Tape and reel

# Contents

- 1      Device block diagram ..... 5**
- 2      Pin description ..... 6**
  - 2.1 Pinout ..... 6
  - 2.2 Pin list ..... 7
- 3      Electrical specifications ..... 8**
  - 3.1 Absolute maximum ratings ..... 8
  - 3.2 Thermal data ..... 8
  - 3.3 Electrical specifications ..... 8
- 4      Characterization curves ..... 10**
  - 4.1 Characterizations for 6 Ω loads with 18 V ..... 10
  - 4.2 Characterizations for 8 Ω loads with 20 V ..... 13
- 5      Applications circuit ..... 17**
- 6      Applications information ..... 18**
  - 6.1 Mode selection ..... 18
  - 6.2 Gain setting ..... 19
  - 6.3 Input resistance and capacitance ..... 19
  - 6.4 Internal and external clocks ..... 20
    - 6.4.1 Master mode (internal clock) ..... 20
    - 6.4.2 Slave mode (external clock) ..... 20
  - 6.5 Output low-pass filter ..... 21
  - 6.6 Protection functions ..... 22
  - 6.7 Diagnostic output ..... 22
- 7      Package mechanical data ..... 23**
- 8      Revision history ..... 25**

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin description list . . . . .	7
Table 3.	Absolute maximum ratings . . . . .	8
Table 4.	Thermal data . . . . .	8
Table 5.	Electrical specifications . . . . .	8
Table 6.	Mode settings . . . . .	18
Table 7.	Gain settings . . . . .	19
Table 8.	How to set up SYNCLK . . . . .	20
Table 9.	PowerSSO-36 EPD dimensions . . . . .	23
Table 10.	Document revision history . . . . .	25

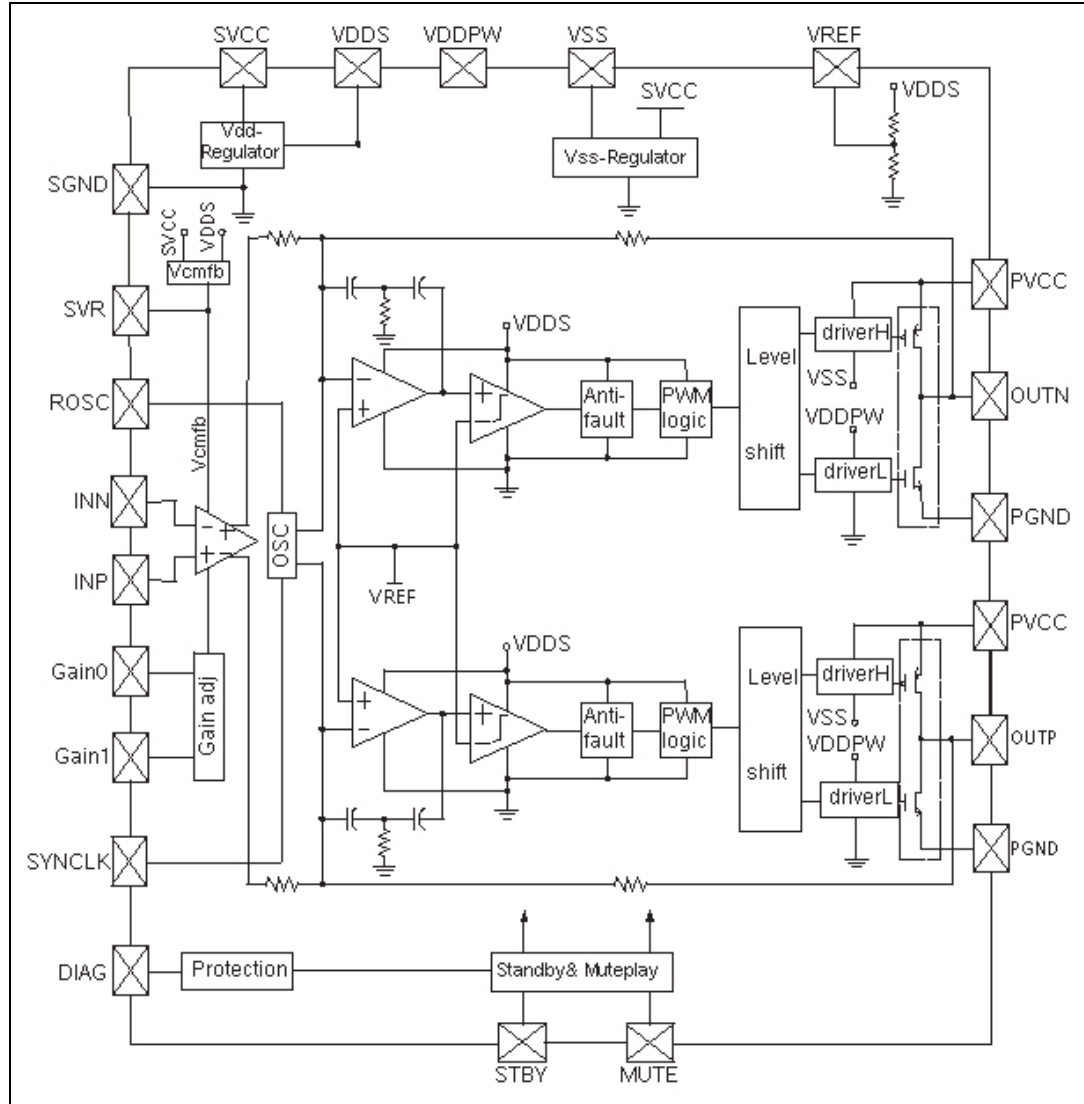
## List of figures

Figure 1.	Internal block diagram (showing one channel only)	5
Figure 2.	Pin connections (top view, PCB view)	6
Figure 3.	Output power vs. supply voltage	10
Figure 4.	THD at 1 kHz vs. output power	10
Figure 5.	THD at 100 Hz vs. output power	11
Figure 6.	THD at 1 W vs. frequency	11
Figure 7.	Frequency response	11
Figure 8.	Crosstalk vs frequency	12
Figure 9.	FFT 0 dB	12
Figure 10.	FFT -60 dB	12
Figure 11.	Output power vs supply voltage	13
Figure 12.	THD at 1 kHz vs output power	13
Figure 13.	THD at 100 Hz vs output power	14
Figure 14.	THD at 1 W vs frequency	14
Figure 15.	Frequency response	14
Figure 16.	Crosstalk vs frequency	15
Figure 17.	FFT 0 dB	15
Figure 18.	FFT -60 dB	15
Figure 19.	Test board (SZ-LAB-TDA7492P) layout	16
Figure 20.	Applications circuit for class-D amplifier	17
Figure 21.	Standby and mute circuits	18
Figure 22.	Turn-on/off sequence for minimizing speaker “pop”	18
Figure 23.	Device input circuit and frequency response	19
Figure 24.	Master and slave connection	20
Figure 25.	Typical LC filter for a 8-Ω speaker	21
Figure 26.	Typical LC filter for a 4-Ω speaker	21
Figure 27.	Behavior of pin DIAG for various protection conditions	22
Figure 28.	PowerSSO-36 EPD outline drawing	24

# 1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7492P.

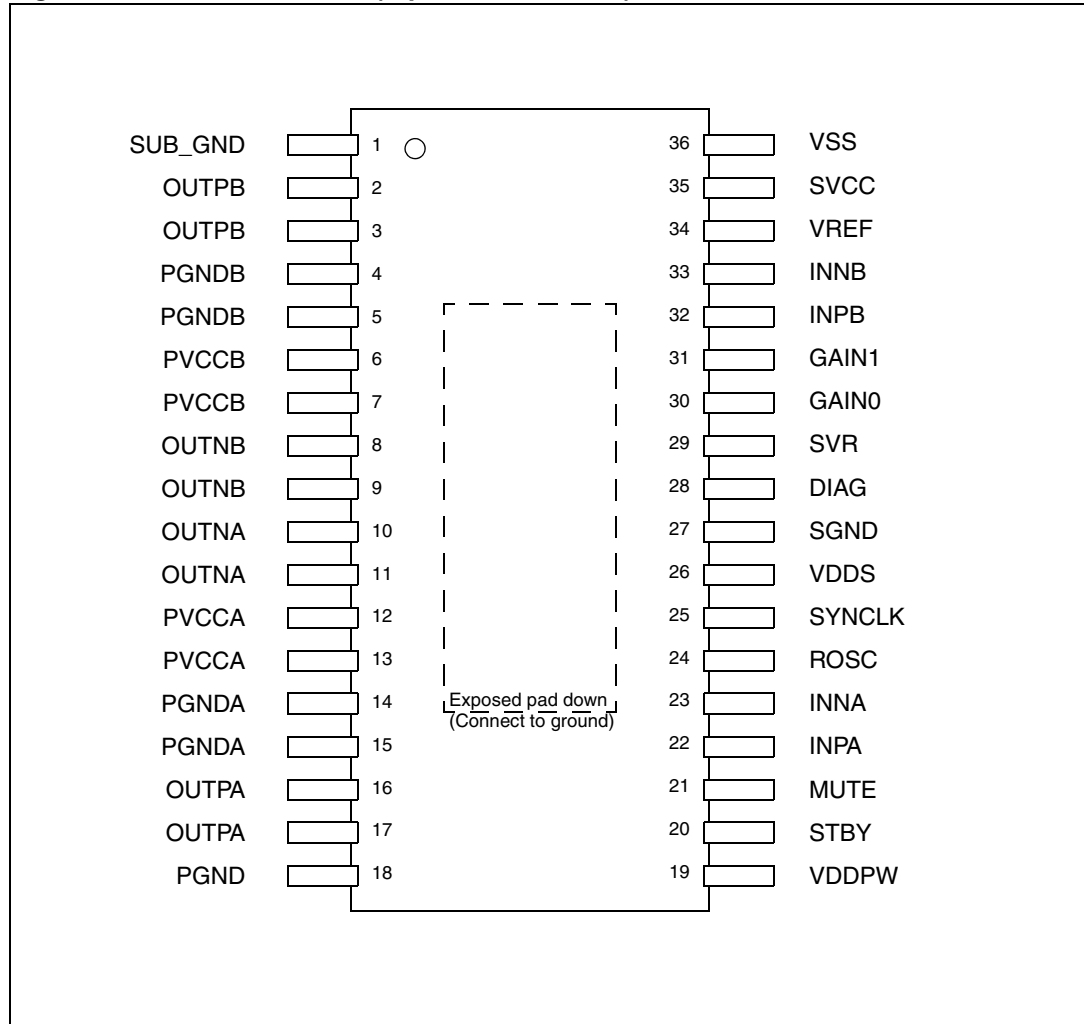
Figure 1. Internal block diagram (showing one channel only)



## 2 Pin description

### 2.1 Pinout

Figure 2. Pin connections (top view, PCB view)



## 2.2 Pin list

**Table 2. Pin description list**

Number	Name	Type	Description
1	SUB_GND	PWR	Connect to the frame
2,3	OUTPB	O	Positive PWM for right channel
4,5	PGNDB	PWR	Power stage ground for right channel
6,7	PVCCB	PWR	Power supply for right channel
8,9	OUTNB	O	Negative PWM output for right channel
10,11	OUTNA	O	Negative PWM output for left channel
12,13	PVCCA	PWR	Power supply for left channel
14,15	PGNDA	PWR	Power stage ground for left channel
16,17	OUTPA	O	Positive PWM output for left channel
18	PGND	PWR	Power stage ground
19	VDDPW	O	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	I	Standby mode control
21	MUTE	I	Mute mode control
22	INPA	I	Positive differential input of left channel
23	INNA	I	Negative differential input of left channel
24	ROSC	O	Master oscillator frequency-setting pin
25	SYNCLK	I/O	Clock in/out for external oscillator
26	VDDS	O	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	PWR	Signal ground
28	DIAG	O	Open-drain diagnostic output
29	SVR	O	Supply voltage rejection
30	GAIN0	I	Gain setting input 1
31	GAIN1	I	Gain setting input 2
32	INPB	I	Positive differential input of right channel
33	INNB	I	Negative differential input of right channel
34	VREF	O	Half VDDS (nominal) referred to ground
35	SVCC	PWR	Signal power supply
36	VSS	O	3.3-V (nominal) regulator output referred to power supply
-	EP	PWR	Exposed pad for connection to ground plane as heatsink

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CCMAX}$	DC supply voltage for pins PVCCA, PVCCB, SVCC	30	V
$V_I$	Voltage limits for input pins STANDBY, MUTE, INNA, INPA, INN B, INPB, GAIN0, GAIN1	-0.3 to 3.6	V
$T_{op}$	Operating temperature	-40 to 85	°C
$T_j$	Junction temperature	-40 to 150	°C
$T_{stg}$	Storage temperature	-40 to 150	°C

### 3.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j-case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j-amb}$	Thermal resistance, junction to ambient	-	24 <sup>(1)</sup>	-	°C/W

1. FR4 with vias to copper area of 9 cm<sup>2</sup>

### 3.3 Electrical specifications

Unless otherwise stated, the results in [Table 5](#) below are given for the conditions:

$V_{CC} = 20\text{ V}$ ,  $R_L$  (load) = 8  $\Omega$ ,  $R_{OSC} = R3 = 39\text{ k}\Omega$ , C8 = 100 nF, f = 1 kHz,  $G_V = 21.6\text{ dB}$ , and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

**Table 5. Electrical specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{CC}$	Supply voltage for pins PVCCA, PVCCB, SVCC	-	8	-	26	V
$I_q$	Total quiescent	-	-	26	35	mA
$I_{qSTBY}$	Quiescent current in standby	-	-	2.5	5.0	$\mu\text{A}$
$V_{OS}$	Output offset voltage	Play mode	-	-	$\pm 100$	mV
		Mute mode	-	-	$\pm 60$	mV
$I_{OCP}$	Overcurrent protection threshold	$R_L = 0\ \Omega$	3.8	4.2	-	A
$T_{jSD}$	Junction temperature at thermal shutdown	-	-	150	-	°C
$R_i$	Input resistance	Differential input	48	60	-	k $\Omega$



Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>OV</sub> P	Overvoltage protection threshold	-	28	29	-	V
V <sub>UV</sub> P	Undervoltage protection threshold	-	-	-	7	V
R <sub>dsON</sub>	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P <sub>o</sub>	Output power	THD = 10%	-	25	-	W
		THD = 1%	-	20	-	
P <sub>o</sub>	Output power	V <sub>CC</sub> = 12 V, THD = 10%	-	9.5	-	W
		V <sub>CC</sub> = 12 V, THD = 1%	-	7.2	-	
P <sub>D</sub>	Power dissipated by device	P <sub>o</sub> = 25 W + 25 W, THD = 10%	-	5.0	-	W
η	Efficiency	P <sub>o</sub> = 10 W + 10 W	80	90	-	%
THD	Total harmonic distortion	P <sub>o</sub> = 1 W	-	0.1	0.4	%
G <sub>V</sub>	Closed-loop gain	GAIN0 = L, GAIN1 = L	20.6	21.6	22.6	dB
		GAIN0 = L, GAIN1 = H	26.6	27.6	28.6	
		GAIN0 = H, GAIN1 = L	30.1	31.1	32.1	
		GAIN0 = H, GAIN1 = H	32.6	33.6	34.6	
ΔG <sub>V</sub>	Gain matching	-	-	±1	dB	
CT	Cross talk	f = 1 kHz	-	50	-	dB
eN	Total input noise	A Curve, G <sub>V</sub> = 20 dB	-	20	-	μV
		f = 22 Hz to 22 kHz	-	25	35	
SVRR	Supply voltage rejection ratio	f <sub>r</sub> = 100 Hz, V <sub>r</sub> = 0.5 V, C <sub>SVR</sub> = 10 μF	40	50	-	dB
T <sub>r</sub> , T <sub>f</sub>	Rise and fall times	-	-	50	-	ns
f <sub>SW</sub>	Switching frequency	Internal oscillator	290	310	330	kHz
f <sub>SWR</sub>	Output switching frequency range	With internal oscillator <sup>(1)</sup>	250	-	400	kHz
		With external oscillator <sup>(2)</sup>	250	-	400	
V <sub>inH</sub>	Digital input high (H)	-	2.3	-	-	V
V <sub>inL</sub>	Digital input low (L)		-	-	0.8	
A <sub>MUTE</sub>	Mute attenuation	V <sub>MUTE</sub> = 1 V	60	80	-	dB

1.  $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$  kHz,  $f_{SYNCLK} = 2 * f_{SW}$  with R3 = 39 kΩ, see [Figure 20](#).

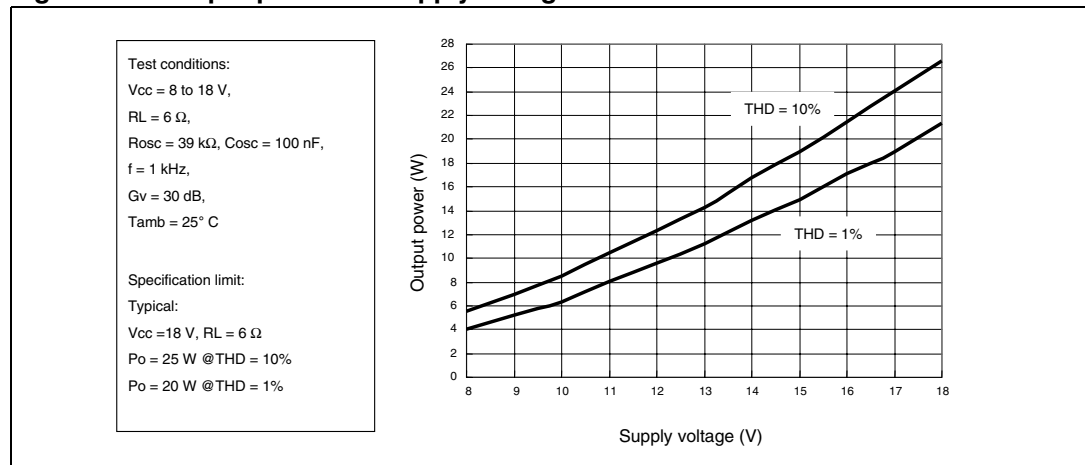
2.  $f_{SW} = f_{SYNCLK} / 2$  with the frequency of the external oscillator.

## 4 Characterization curves

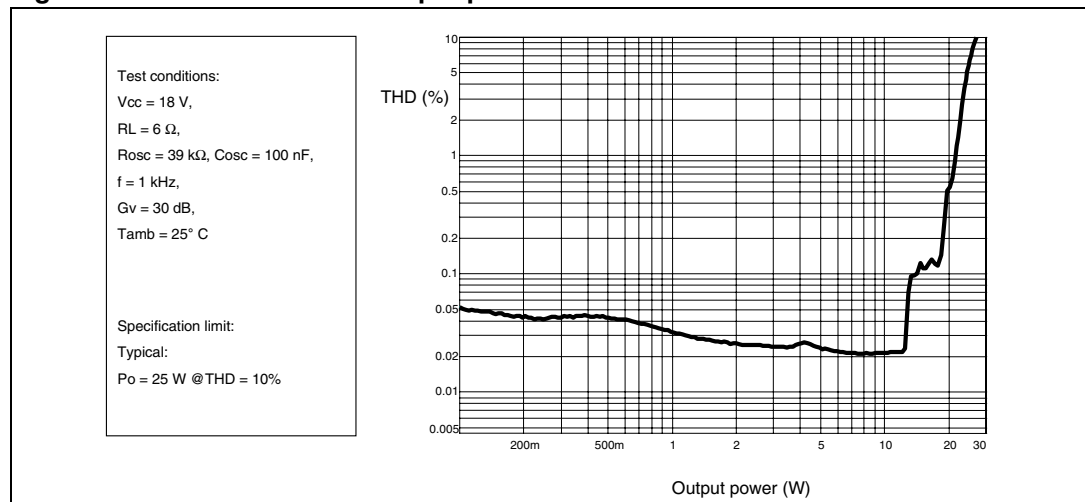
The following characterizations were made using the SZ-LAB-TDA7492P demo board. The layout is shown in [Figure 19 on page 16](#). The LC filter for the 6 Ω load used 22 μH and 220 nF components, whilst that for the 8 Ω load used 33 μH and 220 nF.

### 4.1 Characterizations for 6 Ω loads with 18 V

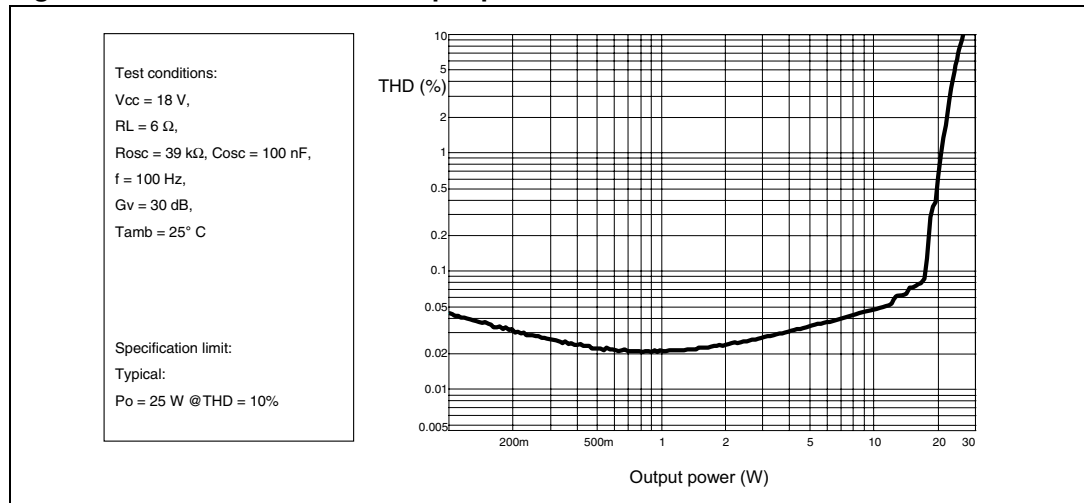
**Figure 3. Output power vs. supply voltage**



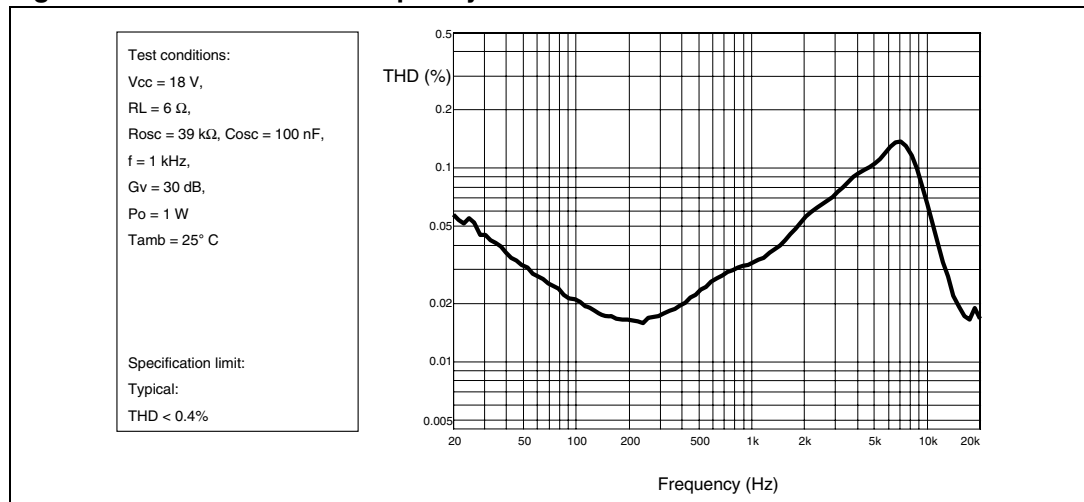
**Figure 4. THD at 1 kHz vs. output power**



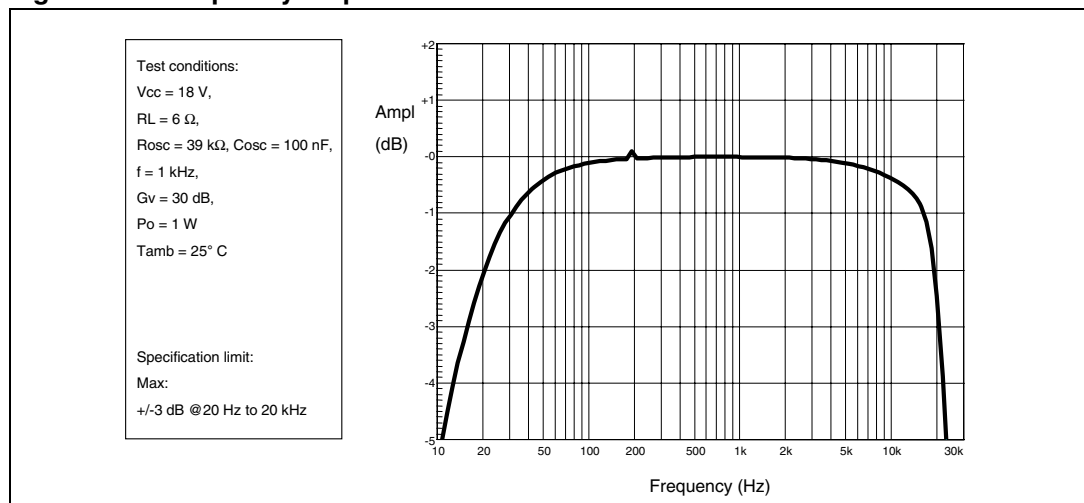
**Figure 5. THD at 100 Hz vs. output power**



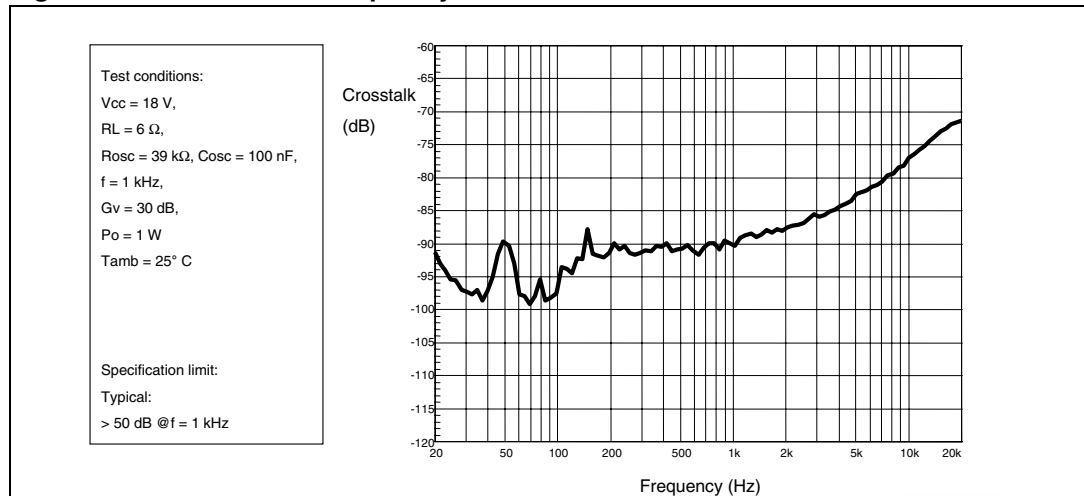
**Figure 6. THD at 1 W vs. frequency**



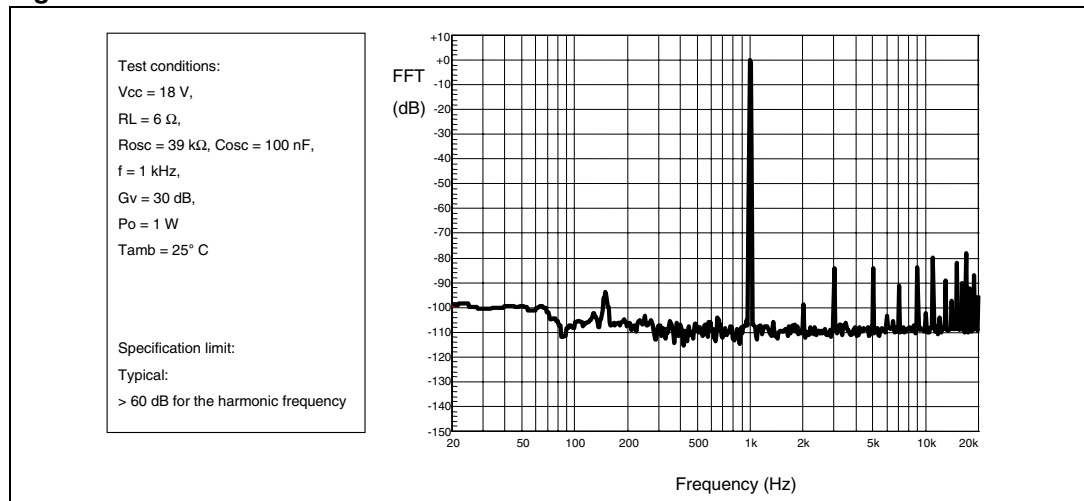
**Figure 7. Frequency response**



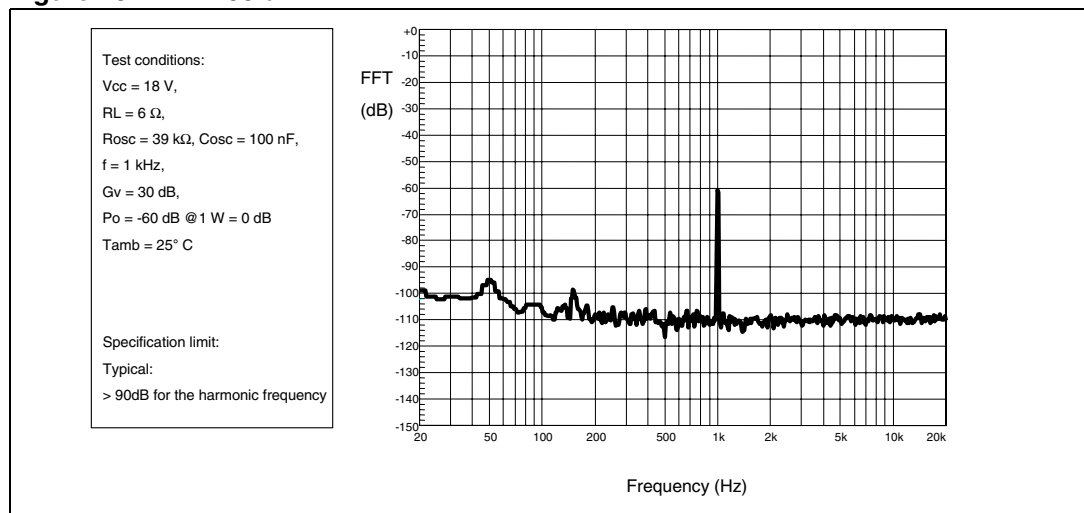
**Figure 8. Crosstalk vs frequency**



**Figure 9. FFT 0 dB**



**Figure 10. FFT -60 dB**



## 4.2 Characterizations for 8 Ω loads with 20 V

Figure 11. Output power vs supply voltage

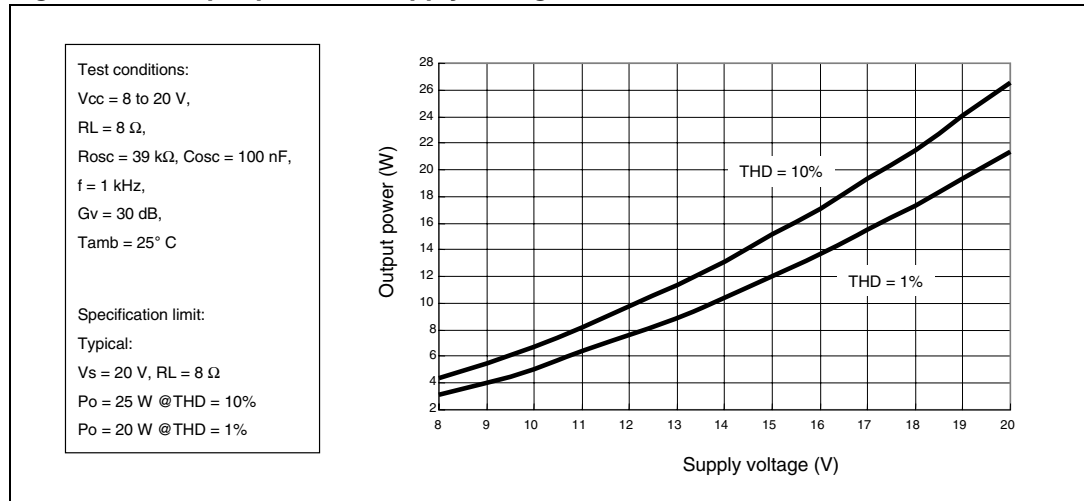


Figure 12. THD at 1 kHz vs output power

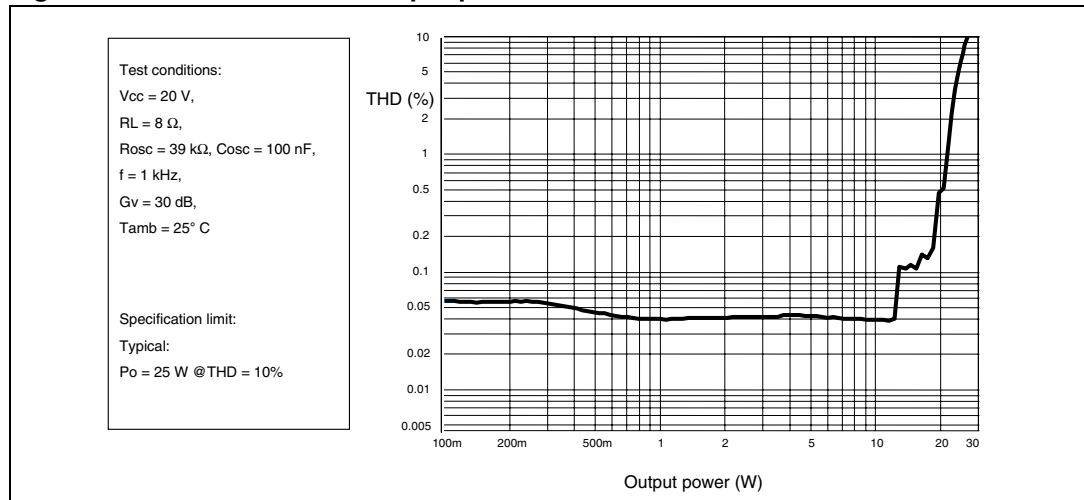


Figure 13. THD at 100 Hz vs output power

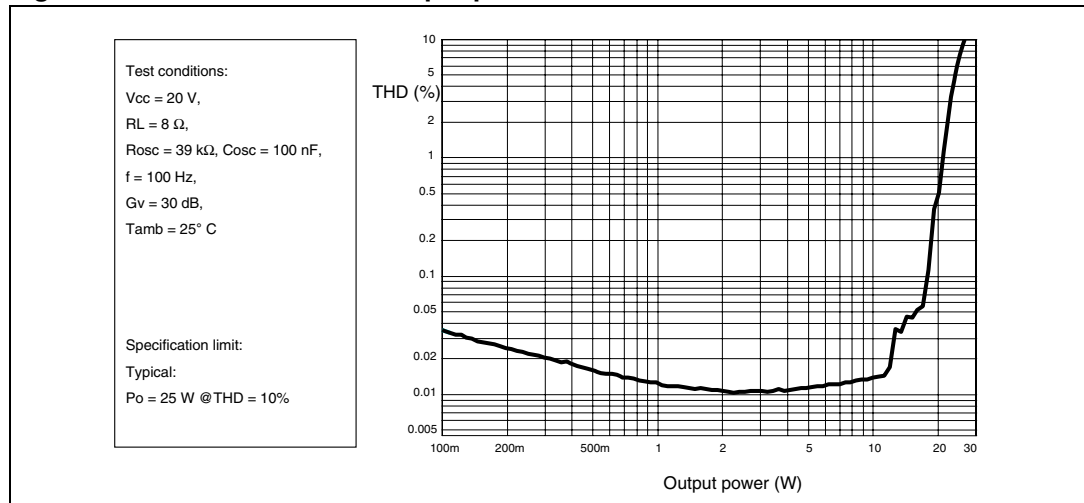


Figure 14. THD at 1 W vs frequency

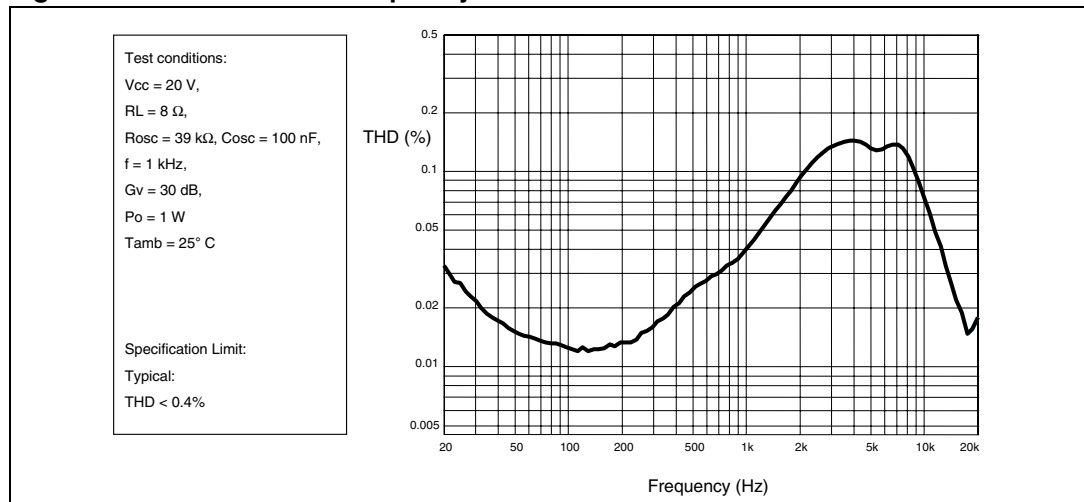
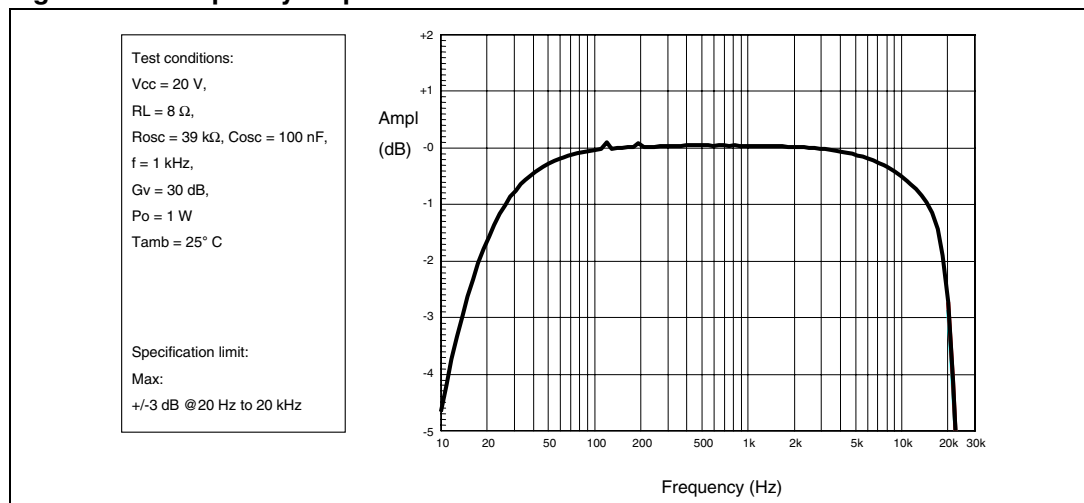
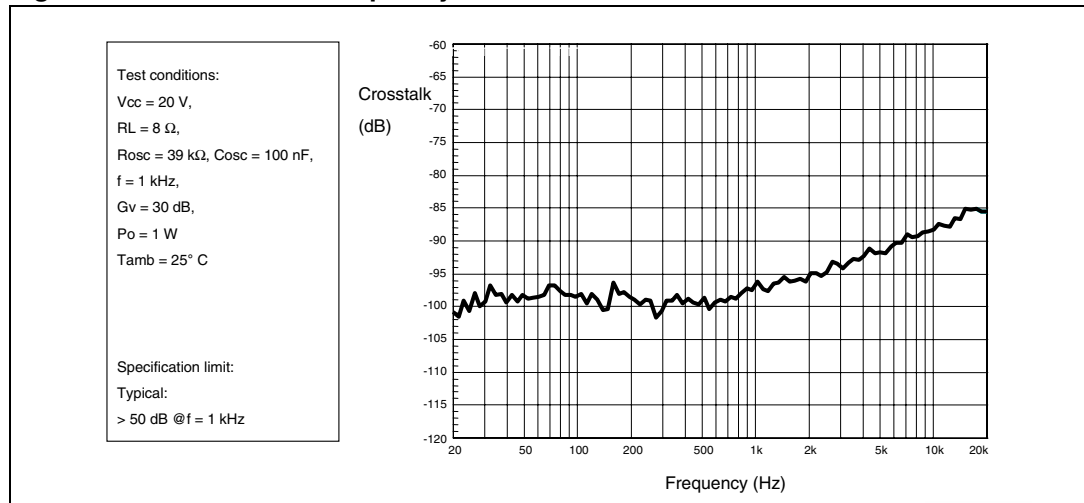


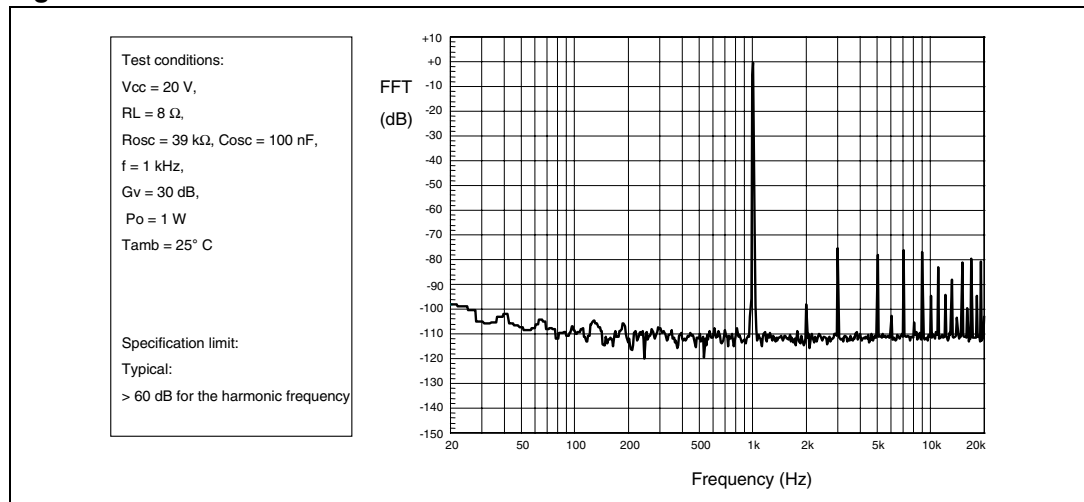
Figure 15. Frequency response



**Figure 16. Crosstalk vs frequency**



**Figure 17. FFT 0 dB**



**Figure 18. FFT -60 dB**

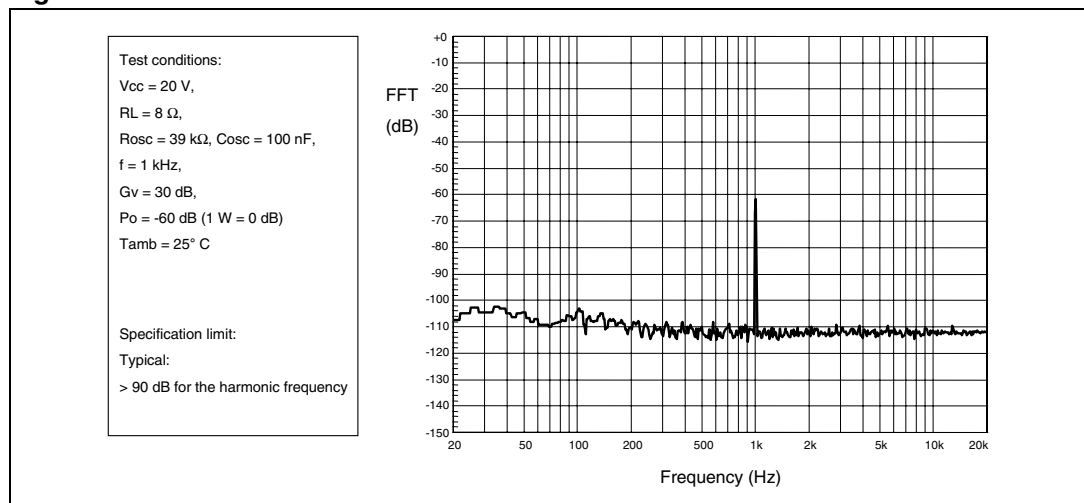
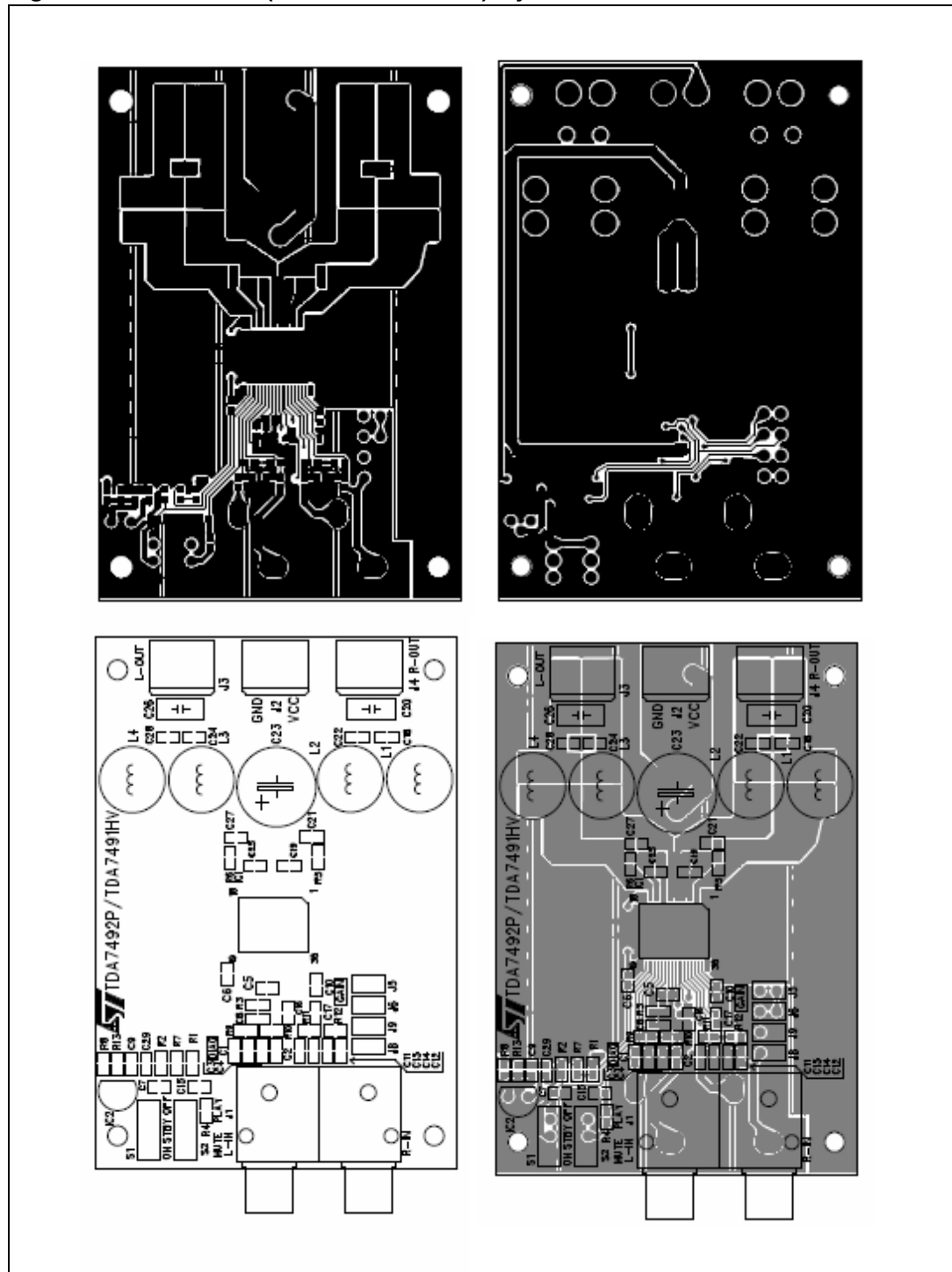


Figure 19. Test board (SZ-LAB-TDA7492P) layout







# 5 Applications circuit

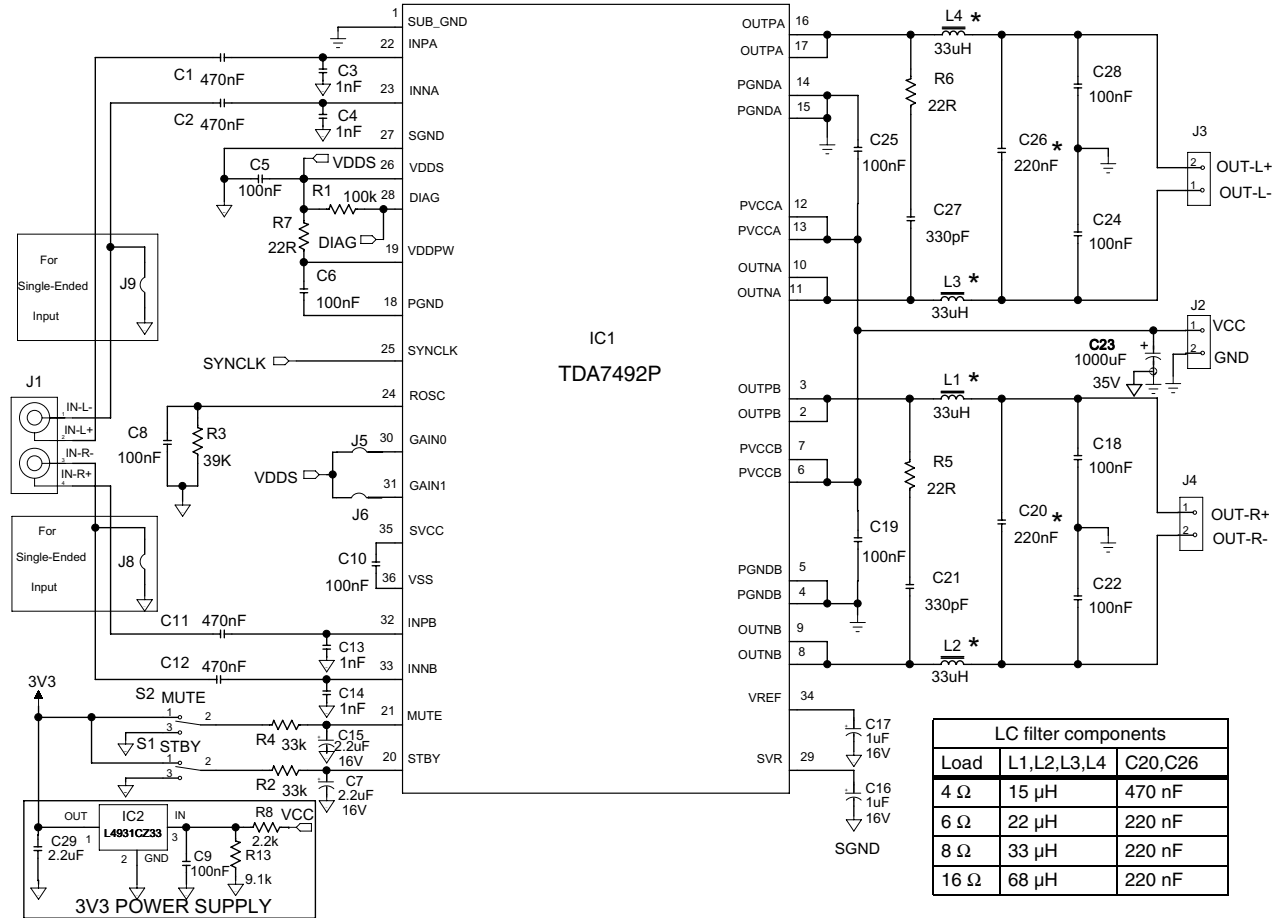
Figure 20. Applications circuit for class-D amplifier

Jumper settings for gain:

GAIN0 : GAIN1	Nominal gain
0 V : 0 V	21.6 dB
0 V : 3.3 V	27.6 dB
3.3 V : 0 V	31.1 dB
3.3 V : 3.3 V	33.6 dB

Switch settings for standby, mute and play:

STBY : MUTE	Mode
0 V : 0 V	Standby
0 V : 3.3 V	Standby
3.3 V : 0 V	Mute
3.3 V : 3.3 V	Play



LC filter components		
Load	L1,L2,L3,L4	C20,C26
4 Ω	15 μH	470 nF
6 Ω	22 μH	220 nF
8 Ω	33 μH	220 nF
16 Ω	68 μH	220 nF

## 6 Applications information

### 6.1 Mode selection

The three operating modes of the TDA7492P are set by the two inputs STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

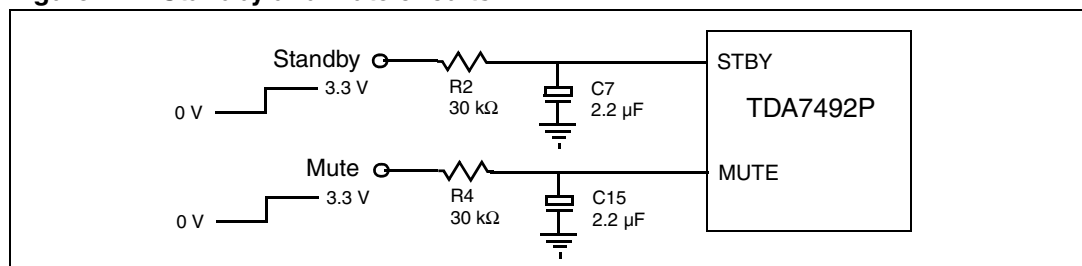
The protection functions of the TDA7492P are enabled by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 21*. The input current of the corresponding pins must be limited to 200  $\mu$ A.

**Table 6. Mode settings**

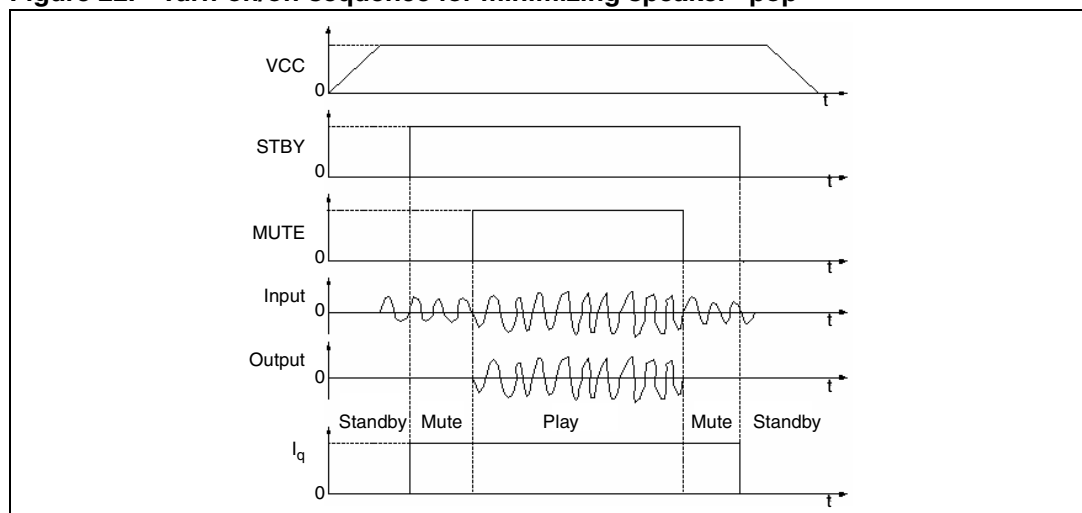
Mode selection	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in *Table 5: Electrical specifications on page 8*

**Figure 21. Standby and mute circuits**



**Figure 22. Turn-on/off sequence for minimizing speaker “pop”**



## 6.2 Gain setting

The gain of the TDA7492P is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin31). Internally, the gain is set by changing the feedback resistors of the amplifier.

**Table 7. Gain settings**

GAIN0	GAIN1	Nominal gain, $G_v$ (dB)
0	0	21.6
0	1	27.6
1	0	31.1
1	1	33.6

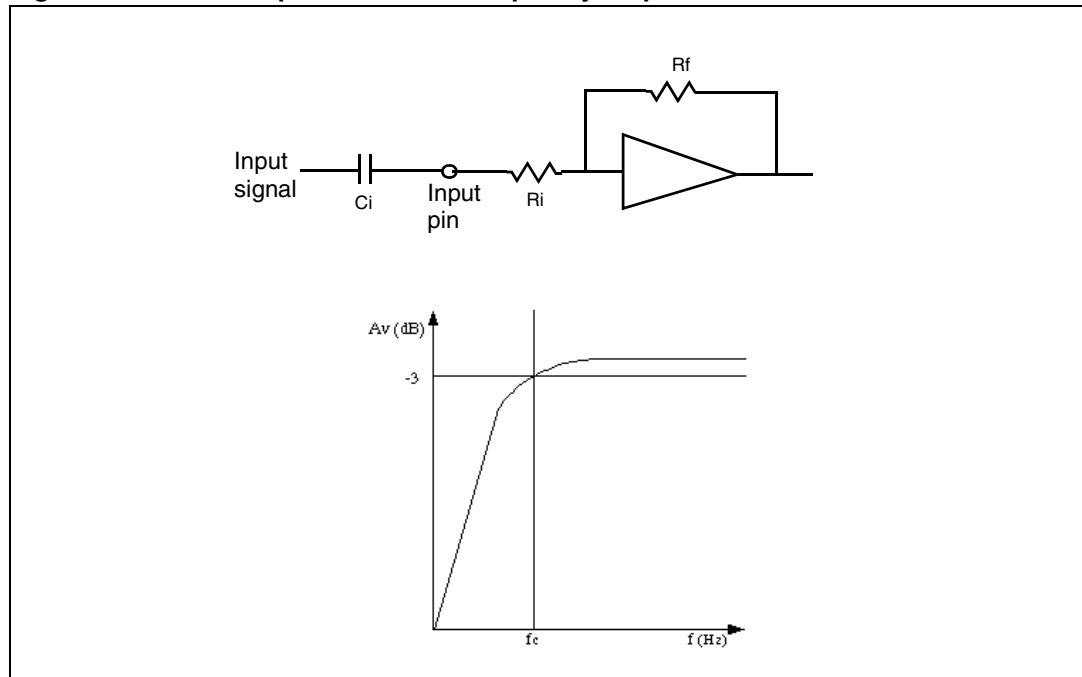
## 6.3 Input resistance and capacitance

The input impedance is set by an internal resistor  $R_i = 60 \text{ k}\Omega$  (typical). An input capacitor ( $C_i$ ) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in [Figure 23](#). For  $C_i = 470 \text{ nF}$  the high-pass filter cutoff frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

**Figure 23. Device input circuit and frequency response**



## 6.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7492P as master clock, while the other devices are in slave mode (that is, externally clocked). The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

### 6.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency,  $f_{SW}$ , is controlled by the resistor,  $R_{OSC}$ , connected to pin ROSC:

$$f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4) \text{ kHz}$$

where  $R_{OSC}$  is in  $k\Omega$ .

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor  $R_{OSC}$  must be less than 60  $k\Omega$  as given below in [Table 8](#).

### 6.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in [Table 8](#).

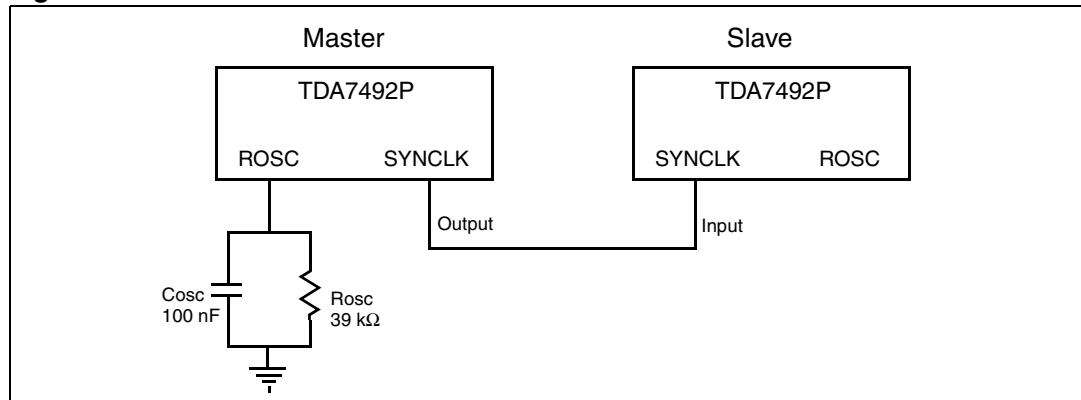
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

**Table 8. How to set up SYNCLK**

Mode	ROSC	SYNCLK
Master	$R_{OSC} < 60 \text{ k}\Omega$	Output
Slave	Floating (not connected)	Input

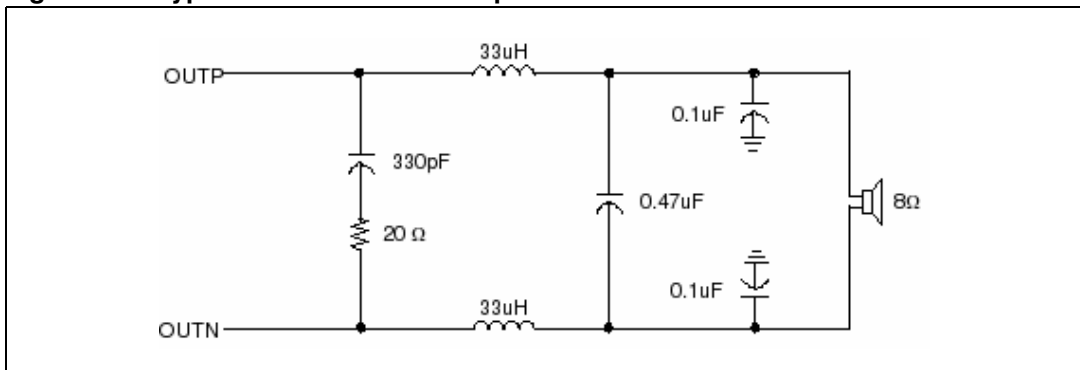
**Figure 24. Master and slave connection**



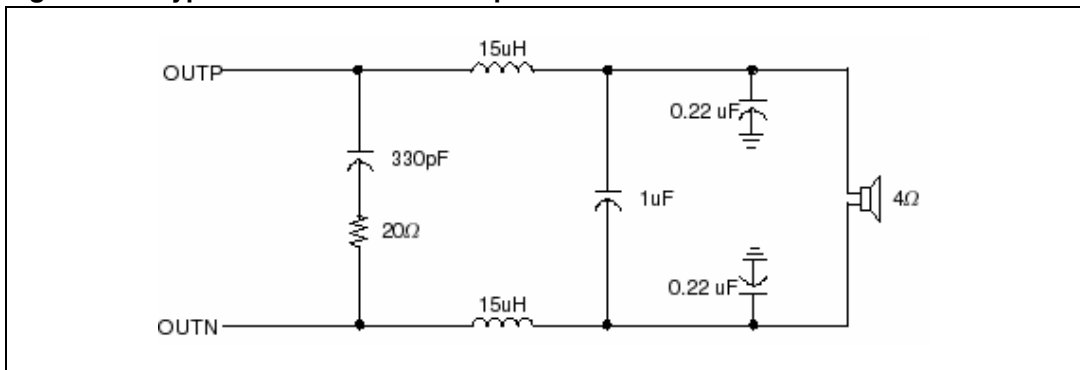
### 6.5 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cutoff frequency of 27 kHz, are shown in [Figure 25](#) and [Figure 26](#) below.

**Figure 25. Typical LC filter for a 8-Ω speaker**



**Figure 26. Typical LC filter for a 4-Ω speaker**



## 6.6 Protection functions

The TDA7492P is fully protected against overvoltages, undervoltages, overcurrents and thermal overloads as explained here.

### Overvoltage protection (OVP)

If the supply voltage exceeds the value for  $V_{OVP}$  given in [Table 5: Electrical specifications on page 8](#) the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

### Undervoltage protection (UVP)

If the supply voltage drops below the value for  $V_{UVP}$  given in [Table 5: Electrical specifications on page 8](#) the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

### Overcurrent protection (OCP)

If the output current exceeds the value for  $I_{OCP}$  given in [Table 5: Electrical specifications on page 8](#) the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time,  $T_{OC}$ , is determined by the R-C components connected to pin STBY.

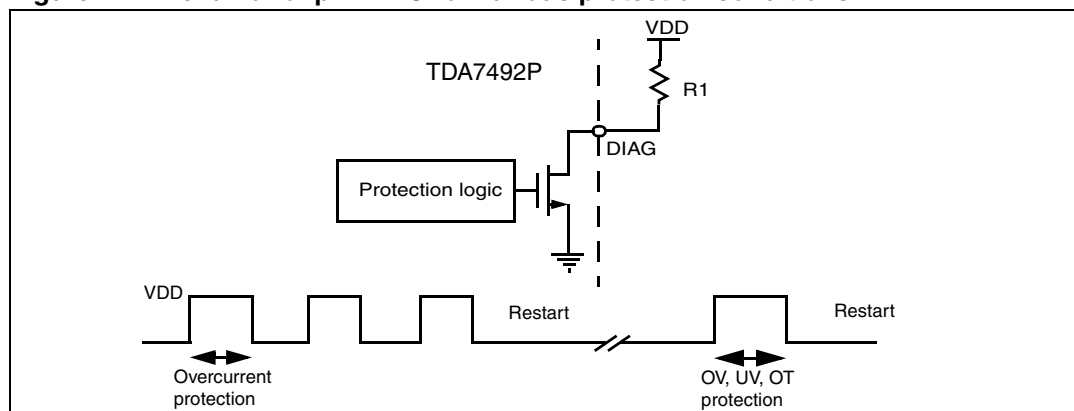
### Thermal protection (OTP)

If the junction temperature,  $T_j$ , reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for  $T_j$  given in [Table 5: Electrical specifications on page 8](#) the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently the device restarts.

## 6.7 Diagnostic output

The output pin DIAG is an open-drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<26 V) by a pull-up resistor whose value is limited by the maximum sinking current (200  $\mu$ A) of the pin.

**Figure 27. Behavior of pin DIAG for various protection conditions**



## 7 Package mechanical data

The TDA7492P comes in a 36-pin PowerSSO package with exposed pad down.

[Figure 28](#) below shows the package outline and [Table 9](#) gives the dimensions.

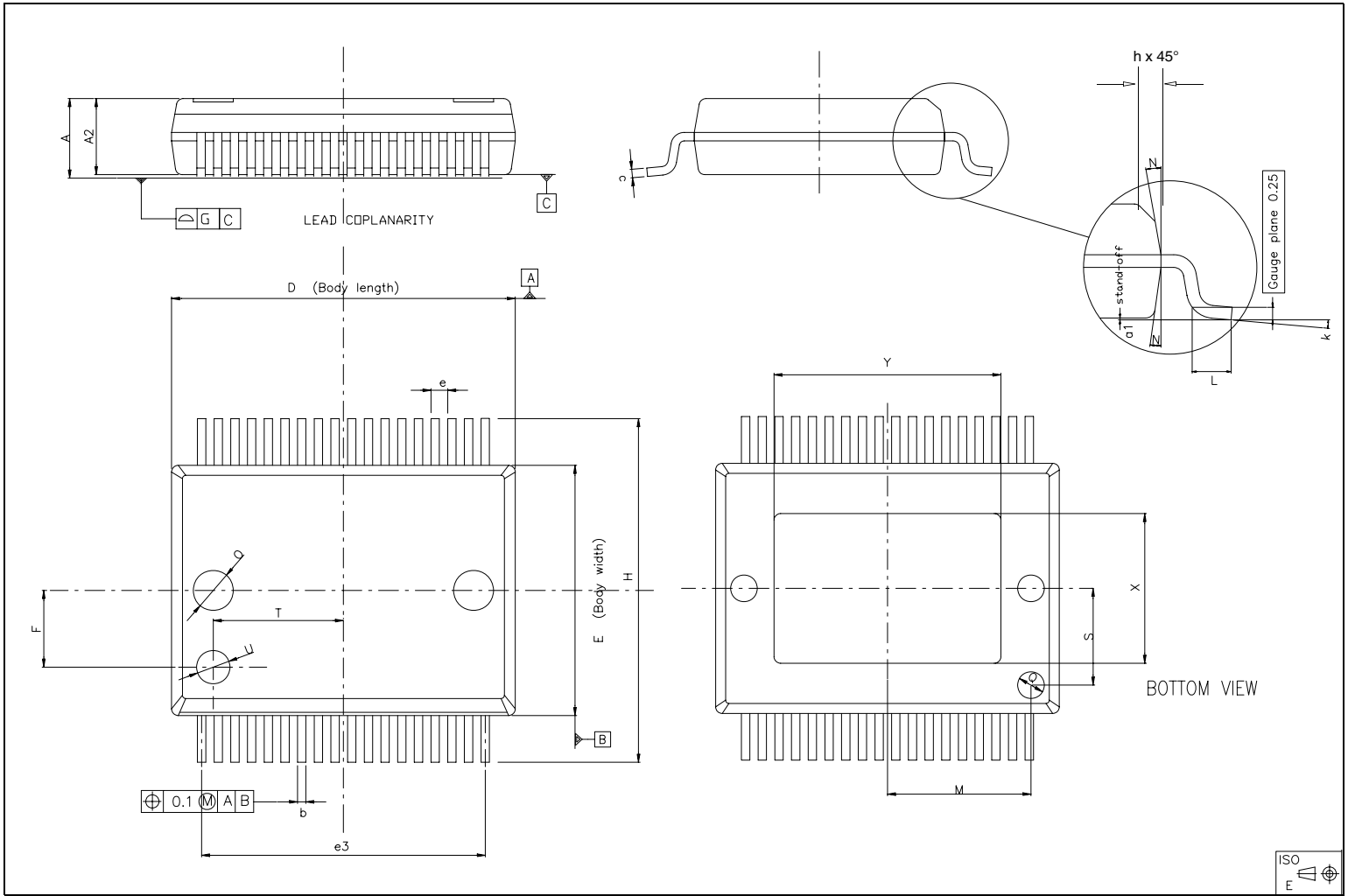
**Table 9. PowerSSO-36 EPD dimensions**

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.45	0.085	-	0.096
A2	2.15	-	2.35	0.085	-	0.093
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



Figure 28. PowerSSO-36 EPD outline drawing





## 8 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
30-Sep-2008	1	Initial release.
11-May-2009	2	Updated supply operating range to 8 V - 26 V <a href="#">on page 1</a> Changed C1 to C8 at beginning of <a href="#">Section 3.3 on page 8</a> Updated <a href="#">Table 5: Electrical specifications on page 8</a> for $V_{CC}$ min, $V_{OS}$ min/max and added new parameter $V_{UV}$ Updated <a href="#">Figure 20: Applications circuit for class-D amplifier on page 17</a> Inserted brackets in equation in <a href="#">Table 5</a> footnote and in <a href="#">Section 6.4.1 on page 20</a> Updated values in UVP and OCP in <a href="#">Section 6.6 on page 22</a> Updated voltage to "<26 V" in <a href="#">Section 6.7 on page 22</a> Updated max dimensions for A and A2 in <a href="#">Table 9: PowerSSO-36 EPD dimensions on page 23</a> .
02-Sep-2009	3	Updated value for $G_V$ at head of <a href="#">Section 3.3 on page 8</a> Updated package Y (Min) dimension in <a href="#">Table 9 on page 23</a> .
19-Jan-2011	4	Updated operating temperature range Updated datasheet presentation.
12-Sep-2011	5	Updated OUTNA in <a href="#">Table 2: Pin description list</a>

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)