

TOSHIBA PHOTOCOUPLER GaAs IRED & PHOTO-IC

TLP2200

ISOLATED BUSS DRIVER

HIGH SPEED LINE RECEIVER

MICROPROCESSOR SYSTEM INTERFACES

MOS FET GATE DRIVER

DIRECT REPLACEMENT FOR HCPL-2200

The Toshiba TLP2200 consists of a GaAs light emitting diode and integrated high gain, high speed photodetector.

This unit is 8-lead DIP package.

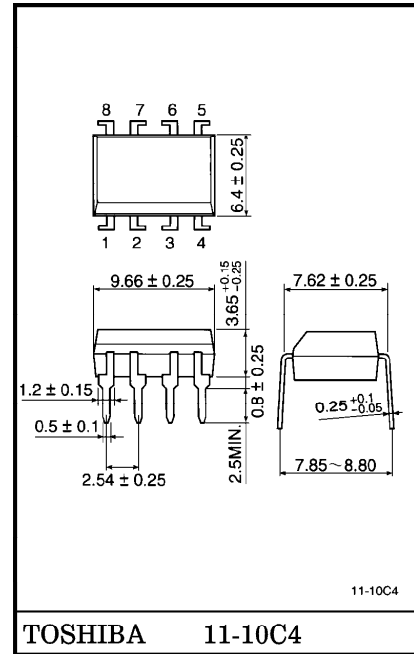
The detector has a three state output stage that eliminates the need for pull-up resistor, and built-in Schmitt trigger. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V / μ s.

- Input Current : $I_F = 1.6\text{mA}$
- Power Supply Voltage : $V_{CC} = 4.5 \sim 20\text{V}$
- Switching Speed : 2.5MBd Guaranteed
- Common Mode Transient Immunity : $\pm 1000\text{V} / \mu\text{s}$ (Min.)
- Guaranteed Performance Over Temp : $0 \sim 85^\circ\text{C}$
- Isolation Voltage : $2500\text{V}_{\text{rms}}$ (Min.)
- UL Recognized : UL1577, File No. E67349

TRUTH TABLE (Positive logic)

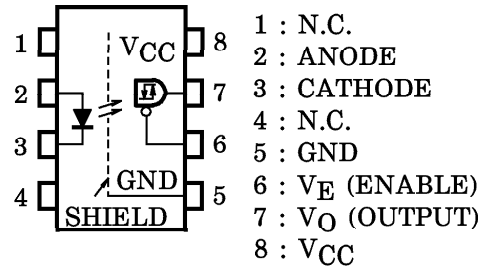
| INPUT | ENABLE | OUTPUT |
|-------|--------|--------|
| H | H | Z |
| L | H | Z |
| H | L | H |
| L | L | L |

Unit in mm

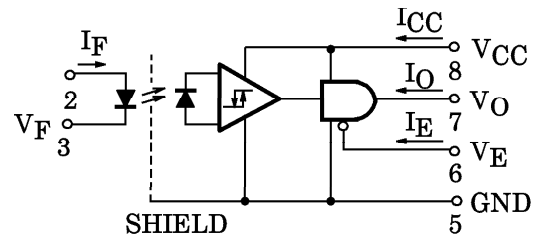


Weight : 0.54g

PIN CONFIGURATION (Top view)



SCHEMATIC



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RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|-----------------------|----------------------|------|------|------|------|
| Input Current, ON | I _F (ON) | 1.6 | — | 5 | mA |
| Input Current, OFF | I _F (OFF) | 0 | — | 0.1 | mA |
| Supply Voltage | V _{CC} | 4.5 | — | 20 | V |
| Enable Voltage High | V _{EH} | 2.0 | — | 20 | V |
| Enable Voltage Low | V _{EL} | 0 | — | 0.8 | V |
| Fan Out (TTL Load) | N | — | — | 4 | — |
| Operating Temperature | T _{opr} | 0 | — | 85 | °C |

ABSOLUTE MAXIMUM RATINGS (No derating required up to 70°C)

| CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|--|------------------|---------|------------------|
| LED | Forward Current | I _F | 10 | mA |
| | Peak Transient Forward Current (Note 1) | I _{FPT} | 1 | A |
| | Reverse Voltage | V _R | 5 | V |
| DETECTOR | Output Current | I _O | 25 | mA |
| | Supply Voltage | V _{CC} | -0.5~20 | V |
| | Output Voltage | V _O | -0.5~20 | V |
| | Three State Enable Voltage | V _E | -0.5~20 | V |
| | Total Package Power Dissipation (Note 2) | P _T | 210 | mW |
| | Operating Temperature Range | T _{opr} | -40~85 | °C |
| Storage Temperature Range | | T _{stg} | -55~125 | °C |
| Lead Solder Temperature (10s) (**) | | T _{sol} | 260 | °C |
| Isolation Voltage (AC 1min., R.H. ≤ 60%, T _a = 25°C) (Note 3) | | BV _S | 2500 | V _{rms} |

(Note 1) Pulse width 1μs 300pps.

(Note 2) Derate 4.5mW/°C above 70°C ambient temperature.

(Note 3) Device considered a two terminal device : pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together

(**) 1.6mm below seating plane.

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- Gallium arsenide (GaAs) is a substance used in the products described in this document. GaAs dust and fumes are toxic. Do not break, cut or pulverize the product, or use chemicals to dissolve them. When disposing of the products, follow the appropriate regulations. Do not dispose of the products with other industrial waste or with domestic garbage.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_a = 0 \sim 85^\circ\text{C}$, $V_{CC} = 4.5 \sim 20\text{V}$,
 $I_F(\text{ON}) = 1.6 \sim 5\text{mA}$, $I_F(\text{OFF}) = 0 \sim 0.1\text{mA}$, $V_{EL} = 0 \sim 0.8\text{V}$, $V_{EH} = 2.0 \sim 20\text{V}$)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | MIN. | TYP.* | MAX. | UNIT | |
|---|---------------------------|--|------------------------------|-----------|-------|----------------------|---------------|
| Output Leakage Current ($V_O > V_{CC}$) | I_{OHH} | $I_F = 5\text{mA}$, $V_{CC} = 4.5\text{V}$ | $V_O = 5.5\text{V}$ | — | — | 100 | μA |
| | | | $V_O = 20\text{V}$ | — | 2 | 500 | |
| Logic Low Output Voltage | V_{OL} | $I_{OL} = 6.4\text{mA}$ (4 TTL load) | — | 0.32 | 0.5 | V | |
| Logic High Output Voltage | V_{OH} | $I_{OH} = -2.6\text{mA}$ | 2.4 | 3.4 | — | V | |
| Logic Low Enable Current | I_{EL} | $V_E = 0.4\text{V}$ | — | -0.13 | -0.32 | mA | |
| Logic High Enable Current | I_{EH} | $V_E = 2.7\text{V}$ | — | — | 20 | μA | |
| | | $V_E = 5.5\text{V}$ | — | — | 100 | | |
| | | $V_E = 20\text{V}$ | — | 0.01 | 250 | | |
| Logic Low Enable Voltage | V_{EL} | — | — | — | 0.8 | V | |
| Logic High Enable Voltage | V_{EH} | — | 2.0 | — | — | V | |
| Logic Low Supply Current | I_{CCL} | $I_F = 0\text{mA}$ $V_E = \text{Don't care}$ | $V_{CC} = 5.5\text{V}$ | — | 5 | 6.0 | mA |
| | | | $V_{CC} = 20\text{V}$ | — | 5.6 | 7.5 | |
| Logic High Supply Current | I_{CCH} | $I_F = 5\text{mA}$ $V_E = \text{Don't care}$ | $V_{CC} = 5.5\text{V}$ | — | 2.5 | 4.5 | mA |
| | | | $V_{CC} = 20\text{V}$ | — | 2.8 | 6.0 | |
| High Impedance State Output Current | I_{OZL} | $I_F = 5\text{mA}$ $V_E = 2\text{V}$ | $V_O = 0.4\text{V}$ | — | 1 | -20 | μA |
| | | | $V_O = 2.4\text{V}$ | — | — | 20 | |
| | $V_O = 5.5\text{V}$ | — | — | 100 | | | |
| | $V_O = 20\text{V}$ | — | 0.01 | 500 | | | |
| Logic Low Short Circuit Output Current (Note 4) | I_{OSL} | $I_F = 0\text{mA}$ | $V_O = V_{CC} = 5.5\text{V}$ | 25 | 55 | — | mA |
| | | | $V_O = V_{CC} = 20\text{V}$ | 40 | 80 | — | |
| Logic High Short Circuit Output Current (Note 4) | I_{OSH} | $I_F = 5\text{mA}$ $V_O = \text{GND}$ | $V_{CC} = 5.5\text{V}$ | -10 | -25 | — | mA |
| | | | $V_{CC} = 20\text{V}$ | -25 | -60 | — | |
| Input Current Hysteresis | I_{HYS} | $V_{CC} = 5\text{V}$ | — | 0.05 | — | mA | |
| Input Forward Voltage | V_F | $I_F = 5\text{mA}$, $T_a = 25^\circ\text{C}$ | — | 1.55 | 1.7 | V | |
| Temperature Coefficient of Forward Voltage | $\Delta V_F / \Delta T_a$ | $I_F = 5\text{mA}$ | — | -2.0 | — | mV/ $^\circ\text{C}$ | |
| Input Reverse Breakdown Voltage | BV_R | $I_R = 10\mu\text{A}$, $T_a = 25^\circ\text{C}$ | 5 | — | — | V | |
| Input Capacitance | C_{IN} | $V_F = 0\text{V}$, $f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$ | — | 45 | — | pF | |
| Resistance (Input-Output) | R_{I-O} | $V_{I-O} = 500\text{V}$ R.H. $\leq 60\%$ (Note 3) | 5×10^{10} | 10^{14} | — | Ω | |
| Capacitance (Input-Output) | C_{I-O} | $V_{I-O} = 0\text{V}$, $f = 1\text{MHz}$ (Note 3) | — | 0.6 | — | pF | |

(**) All typ. values are at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_F(\text{ON}) = 3\text{mA}$ unless otherwise specified.

SWITCHING CHARACTERISTICS

(Unless otherwise specified, $T_a = 0 \sim 85^\circ\text{C}$, $V_{CC} = 4.5 \sim 20\text{V}$, $I_F(\text{ON}) = 1.6 \sim 5\text{mA}$, $I_F(\text{OFF}) = 0 \sim 0.1\text{mA}$)

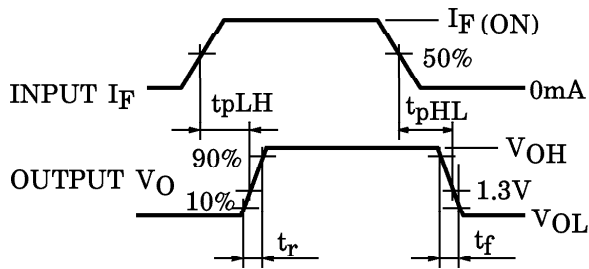
| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|-----------|---------------|--|-------|------|------|--------------------------|
| Propagation Delay Time to Logic High Output Level (Note 5) | t_{pLH} | 1 | Without peaking capacitor C_1 | — | 235 | — | ns |
| | | | With peaking capacitor C_1 | — | — | 400 | |
| Propagation Delay Time to Logic Low Output Level (Note 5) | t_{pHL} | | Without peaking capacitor C_1 | — | 250 | — | ns |
| | | | With peaking capacitor C_1 | — | — | 400 | |
| Output Rise Time (10-90%) | t_r | | — | — | 35 | — | ns |
| Output Fall Time (90-10%) | t_f | | — | — | 20 | — | ns |
| Output Enable Time to Logic High | t_{pZH} | 2 | — | — | — | ns | |
| Output Enable Time to Logic Low | t_{pZL} | | — | — | — | ns | |
| Output Disable Time from Logic High | t_{pHZ} | | — | — | — | ns | |
| Output Disable Time from Logic Low | t_{pLZ} | | — | — | — | ns | |
| Common Mode Transient Immunity at Logic High Output (Note 6) | CM_H | 3 | $I_F = 1.6\text{mA}$, $V_{CM} = 50\text{V}$, $T_a = 25^\circ\text{C}$ | -1000 | — | — | $\text{V} / \mu\text{s}$ |
| Common Mode Transient Immunity at Logic Low Output (Note 6) | CM_L | | $I_F = 0\text{mA}$, $V_{CM} = 50\text{V}$, $T_a = 25^\circ\text{C}$ | 1000 | — | — | $\text{V} / \mu\text{s}$ |

(*) ALL Typ. values are at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_F(\text{ON}) = 3\text{mA}$ unless otherwise specified.

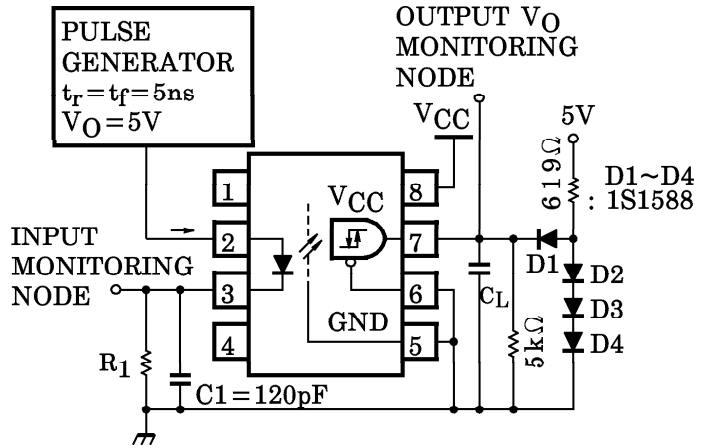
(Note 4) Duration of output short circuit time should not exceed 10ms.

(Note 5) The t_{pLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse.
The t_{pHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.(Note 6) CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O \leq 0.8\text{V}$).
 CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O \leq 2.0\text{V}$).

TEST CIRCUIT 1 t_{pHL} , t_{pLH} , t_r and t_f



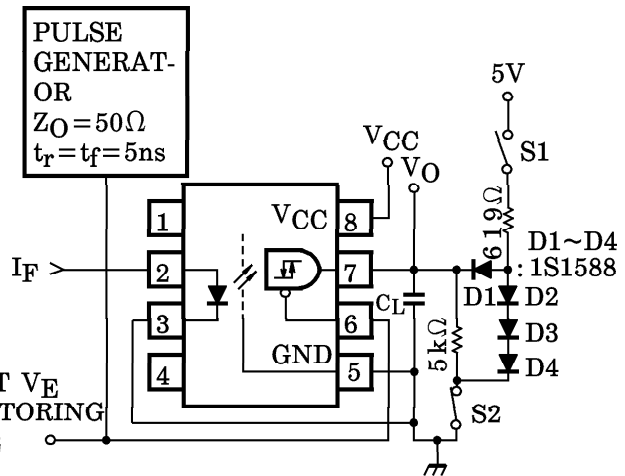
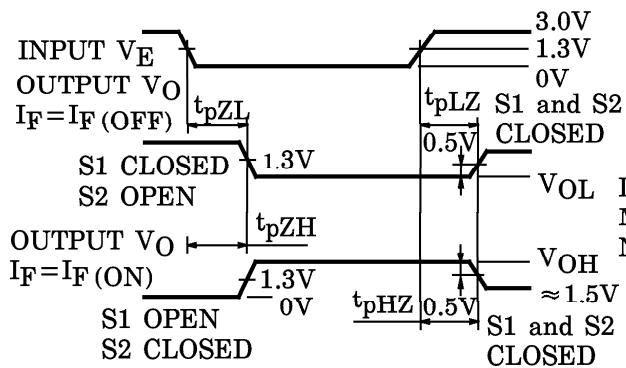
| | | | |
|------------|----------------|---------------|--------------|
| R_1 | 2.15k Ω | 1.1k Ω | 681 Ω |
| I_F (ON) | 1.6mA | 3mA | 5mA |



C_1 is peaking capacitor. The probe and jig capacitances are include in C_1 .

C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2 t_{pHZ} , t_{pZH} , t_{pLZ} and t_{pZL}



C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 3 Common mode transient immunity

