

μ A78L00 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS010S – JANUARY 1976 – REVISED FEBRUARY 2004

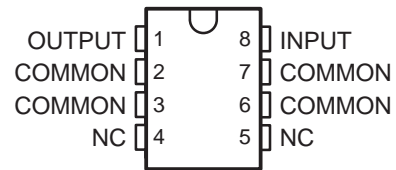
- 3-Terminal Regulators
- Output Current Up To 100 mA
- No External Components
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current Limiting

description/ordering information

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal-shutdown features of these regulators essentially make them immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained, together with lower bias current.

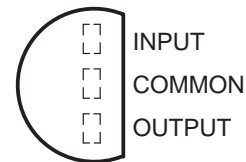
The μ A78L00C and μ A78L00AC series are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The μ A78L05AI is characterized for operation over the virtual junction temperature range of -40°C to 125°C.

**D PACKAGE
(TOP VIEW)**

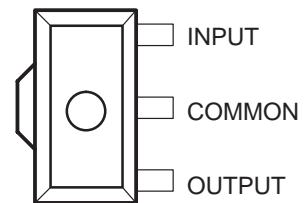


NC – No internal connection

**LP PACKAGE
(TO-92, TO-226AA)
(TOP VIEW)**



**PK PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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description/ordering information (continued)

ORDERING INFORMATION

T _J	V _{O(NOM)} (V)	OUTPUT VOLTAGE TOLERANCE	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	2.6 V	5%	SOIC (D)	Tube of 75	μA78L02ACD	78L02A
			TO-226/TO-92 (LP)	Bulk of 1000	μA78L02ACL P	78L02AC
	5 V	5%	SOIC (D)	Tube of 75	μA78L05ACD	78L05A
				Reel of 2500	μA78L05ACDR	
			SOT-89 (PK)	Reel of 1000	μA78L05ACPK	F5
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μA78L05ACL P	78L05AC
		Pack of 2000		μA78L05ACLPM		
		10%	SOIC (D)	Tube of 75	μA78L05CD	78L05C
				Reel of 2500	μA78L05CDR	
			SOT-89 (PK)	Tube of	μA78L05CPK	B5
	TO-92 (LP) TO-226AA (LP)		Bulk of 1000	μA78L05CLP	78L05C	
		Reel of 2000	μA78L05CLPR			
	6.2 V	5%	SOT-89 (PK)	Reel of 1000	μA78L06ACPK	F6
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μA78L06ACL P	78L06AC
	Reel of 2000	μA78L06ACLPR				
	8 V	5%	SOIC (D)	Tube of 75	μA78L08ACD	78L08A
				Reel of 2500	μA78L08ACDR	78L08A
			SOT-89 (PK)	Reel of 1000	μA78L08ACPK	F8
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μA78L08ACL P	78L08AC
		Reel of 2000		μA78L08ACLPR		
		10%	SOIC (D)	Tube of 75	μA78L08CD	78L08C
	Reel of 2500			μA78L08CDR		
	9 V	5%	SOIC (D)	Tube of 75	μA78L09ACD	78L09A
				Reel of 2500	μA78L09ACDR	
			SOT-89 (PK)	Reel of 1000	μA78L09ACPK	F9
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μA78L09ACL P	78L09AC
	Reel of 2000	μA78L09ACLPR				
	10 V	5%	SOIC (D)	Tube of 75	μA78L10ACD	78L10A
				Reel of 2500	μA78L10ACDR	
			SOT-89 (PK)	Reel of 1000	μA78L10ACPK	FA
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μA78L10ACL P	78L10AC
	Reel of 2000	μA78L10ACLPR				
12 V	5%	SOIC (D)	Tube of 75	μA78L12ACD	78L12A	
			Reel of 2500	μA78L12ACDR		
		SOT-89 (PK)	Reel of 1000	μA78L12ACPK	FC	
		TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μA78L12ACL P	78L12AC	
			Pack of 2000	μA78L12ACLPM		
		Reel of 2000	μA78L12ACLPR			

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



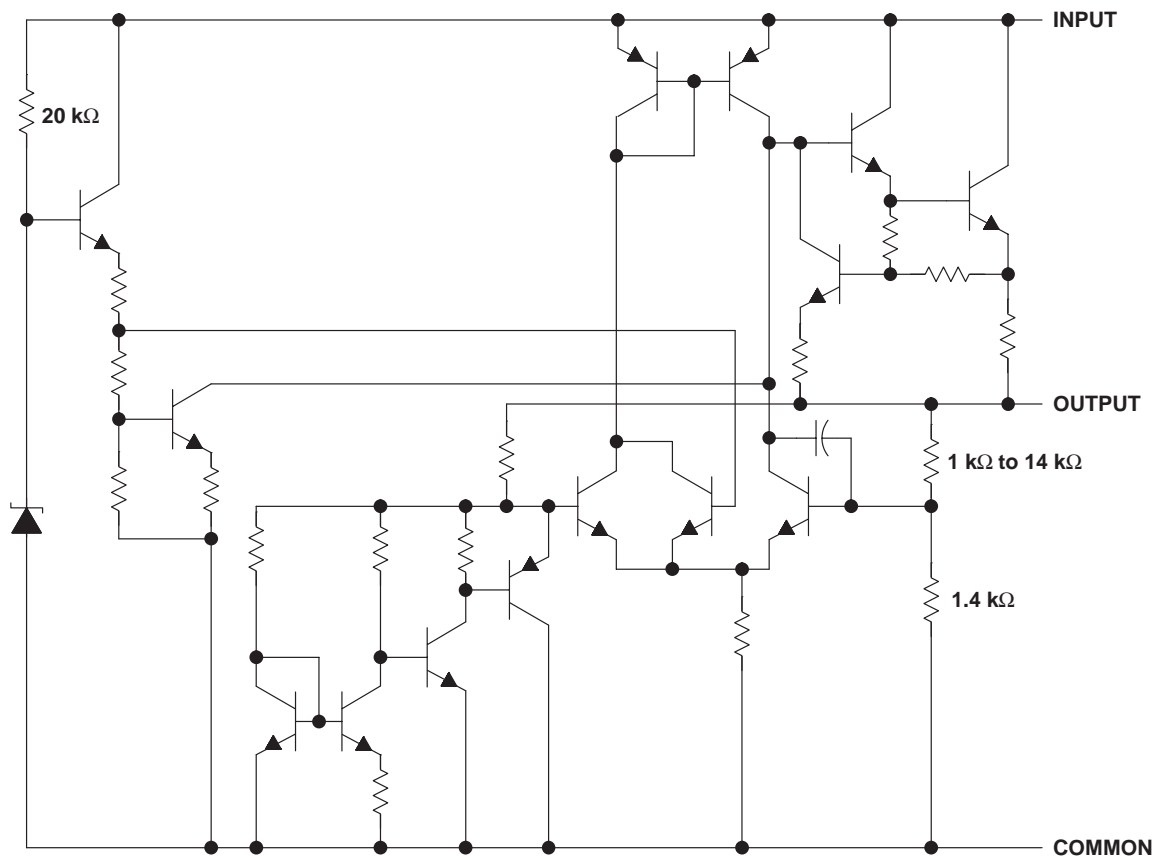
description/ordering information (continued)

ORDERING INFORMATION (continued)

T_J	$V_{O(NOM)}$ (V)	OUTPUT VOLTAGE TOLERANCE	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	15 V	5%	SOIC (D)	Tube of 75	μA78L15ACD	78L15A
				Reel of 2500	μA78L15ACDR	
			SOT-89 (PK)	Reel of 1000	μA78L15ACPK	FF
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000 Reel of 2000	μA78L15ACL μA78L15ACLPR	78L15AC
-40°C to 125°C	5 V	5%	SOIC (D)	Tube of 75	μA78L05AID	78L15AI
				Reel of 2500	μA78L05AIDR	
			SOT-89 (PK)	Reel of 1000	μA78L05AIPK	J5
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000 Reel of 2000	μA78L05AIL μA78L05AILPR	78L05AI

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic



NOTE A: Resistor values shown are nominal.

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absolute maximum ratings over virtual junction temperature range (unless otherwise noted)†

Input voltage, V_I : μA78L02AC, μA78L05C–μA78L09C, μA78L10AC	30 V
μA78L12C, μA78L12AC, μA78L15C, μA78L15AC	35 V
Virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ_{JC}	θ_{JA}
SOIC (D)	High K, JESD 51-7	39°C/W	97°C/W
TO-92/TO-226AA (LP)	High K, JESD 51-7	55°C/W	140°C/W
SOT-89 (PK)	High K, JESD 51-7	9°C/W	52°C/W

NOTE 1: Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT	
V_I	Input voltage	μA78L02AC	4.75	20	V
		μA78L05C, μA78L05AC	7	20	
		μA78L06C, μA78L06AC	8.5	20	
		μA78L08C, μA78L08AC	10.5	23	
		μA78L09C, μA78L09AC	11.5	24	
		μA78L10AC	12.5	25	
		μA78L12C, μA78L12AC	14.5	27	
	μA78L15C, μA78L15AC	17.5	30		
I_O	Output current		100	mA	
T_J	Operating virtual junction temperature range	μA78LxxC and μA78LxxAC series	0	125	°C
		μA78L05AI	–40	125	



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electrical characteristics at specified virtual junction temperature, $V_I = 9\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L02AC			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 4.75\text{ V to }20\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	2.5	2.6	2.7	V
		0°C to 125°C	2.45		2.75	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	2.45		2.75	
Input voltage regulation	$V_I = 4.75\text{ V to }20\text{ V}$	25°C		20	100	mV
	$V_I = 5\text{ V to }20\text{ V}$			16	75	
Ripple rejection	$V_I = 6\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$	25°C	43	51		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		12	50	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			6	25	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		30		μV
Dropout voltage		25°C		1.7		V
Bias current		25°C		3.6	6	mA
		125°C			5.5	
Bias current change	$V_I = 5\text{ V to }20\text{ V}$	0°C to 125°C			2.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J ‡	μA78L05C			μA78L05AC μA78L05AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 7\text{ V to }20\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	4.6	5	5.4	4.8	5	5.2	V
		Full range	4.5		5.5	4.75		5.25	
	$I_O = 1\text{ mA to }70\text{ mA}$	Full range	4.5		5.5	4.75		5.25	
Input voltage regulation	$V_I = 7\text{ V to }20\text{ V}$	25°C		32	200		32	150	mV
	$V_I = 8\text{ V to }20\text{ V}$			26	150		26	100	
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	25°C	40	49		41	49		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		15	60		15	60	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			8	30		8	30	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		42		42			μV
Dropout voltage		25°C		1.7		1.7			V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 8\text{ V to }20\text{ V}$	Full range			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

‡ Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Full range for the μA78L05AC is $T_J = 0^\circ\text{C to }125^\circ\text{C}$, and full range for the μA78L05AI is $T_J = -40^\circ\text{C to }125^\circ\text{C}$.



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electrical characteristics at specified virtual junction temperature, $V_I = 12\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L06C			μA78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 8.5\text{ V to }20\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	5.7	6.2	6.7	5.95	6.2	6.45	V
		0°C to 125°C	5.6		6.8	5.9		6.5	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	5.6		6.8	5.9		6.5	
Input voltage regulation	$V_I = 8.5\text{ V to }20\text{ V}$	25°C	35		200	35		175	mV
	$V_I = 9\text{ V to }20\text{ V}$		29		150	29		125	
Ripple rejection	$V_I = 10\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$	25°C	39	48		40	48	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C	16		80	16		80	mV
	$I_O = 1\text{ mA to }40\text{ mA}$		9		40	9		40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	46			46			μV
Dropout voltage		25°C	1.7			1.7			V
Bias current		25°C	3.9		6	3.9		6	mA
		125°C			5.5	5.5			
Bias current change	$V_I = 9\text{ V to }20\text{ V}$	0°C to 125°C			1.5	1.5		mA	
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2	0.1			

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L08C			μA78L08AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 10.5\text{ V to }23\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	7.36	8	8.64	7.7	8	8.3	V
		0°C to 125°C	7.2		8.8	7.6		8.4	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	7.2		8.8	7.6		8.4	
Input voltage regulation	$V_I = 10.5\text{ V to }23\text{ V}$	25°C	42		200	42		175	mV
	$V_I = 11\text{ V to }23\text{ V}$		36		150	36		125	
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$	25°C	36	46		37	46	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C	18		80	18		80	mV
	$I_O = 1\text{ mA to }40\text{ mA}$		10		40	10		40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	54			54			μV
Dropout voltage		25°C	1.7			1.7			V
Bias current		25°C	4		6	4		6	mA
		125°C			5.5	5.5			
Bias current change	$V_I = 11\text{ V to }23\text{ V}$	0°C to 125°C			1.5	1.5		mA	
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2	0.1			

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 16\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L09C			μA78L09AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 12\text{ V to }24\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	8.3	9	9.7	8.6	9	9.4	V
		0°C to 125°C	8.1		9.9	8.55		9.45	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	8.1		9.9	8.55		9.45	
Input voltage regulation	$V_I = 12\text{ V to }24\text{ V}$	25°C		45	225		45	175	mV
	$V_I = 13\text{ V to }24\text{ V}$			40	175		40	125	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	25°C	36	45		38	45		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		19	90		19	90	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			11	40		11	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		58		58			μV
Dropout voltage		25°C		1.7		1.7			V
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 13\text{ V to }24\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L10AC			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 13\text{ V to }25\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5		10.5	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	9.5		10.5	
Input voltage regulation	$V_I = 13\text{ V to }25\text{ V}$	25°C		51	175	mV
	$V_I = 14\text{ V to }25\text{ V}$			42	125	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	25°C	37	44		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		20	90	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			11	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		62		μV
Dropout voltage		25°C		1.7		V
Bias current		25°C		4.2	6	mA
		125°C			5.5	
Bias current change	$V_I = 14\text{ V to }25\text{ V}$	0°C to 125°C			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L12C			μA78L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 14\text{ V to }27\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	11.1	12	12.9	11.5	12	12.5	V
		0°C to 125°C	10.8		13.2	11.4		12.6	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	10.8		13.2	11.4		12.6	
Input voltage regulation	$V_I = 14.5\text{ V to }27\text{ V}$	25°C		55	250		55	250	mV
	$V_I = 16\text{ V to }27\text{ V}$			49	200		49	200	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	25°C	36	42		37	42	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		22	100		22	100	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			13	50		13	50	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		70		70		μV	
Dropout voltage		25°C		1.7		1.7		V	
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C			6			6	
Bias current change	$V_I = 16\text{ V to }27\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L15C			μA78L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 17.5\text{ V to }30\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	13.8	15	16.2	14.4	15	15.6	V
		0°C to 125°C	13.5		16.5	14.25		15.75	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	13.5		16.5	14.25		15.75	
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$	25°C		65	300		65	300	mV
	$V_I = 20\text{ V to }30\text{ V}$			58	250		58	250	
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$, $f = 120\text{ Hz}$	25°C	33	39		34	39	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		25	150		25	150	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			15	75		15	75	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		82		82		μV	
Dropout voltage		25°C		1.7		1.7		V	
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C			6			6	
Bias current change	$V_I = 10\text{ V to }30\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



APPLICATION INFORMATION

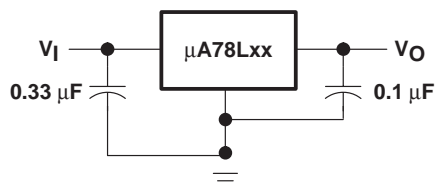


Figure 1. Fixed-Output Regulator

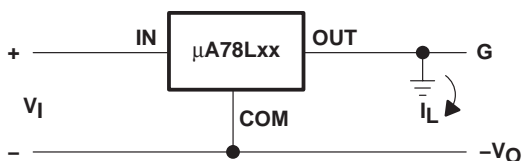


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

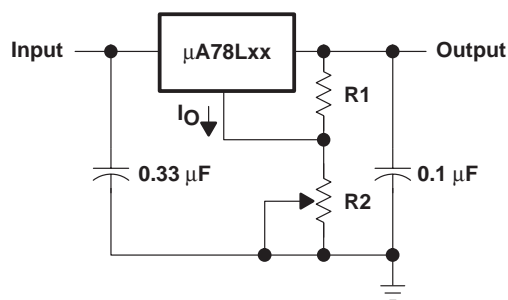


Figure 3. Adjustable-Output Regulator

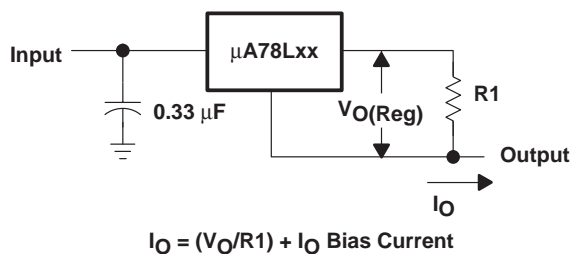


Figure 4. Current Regulator

APPLICATION INFORMATION

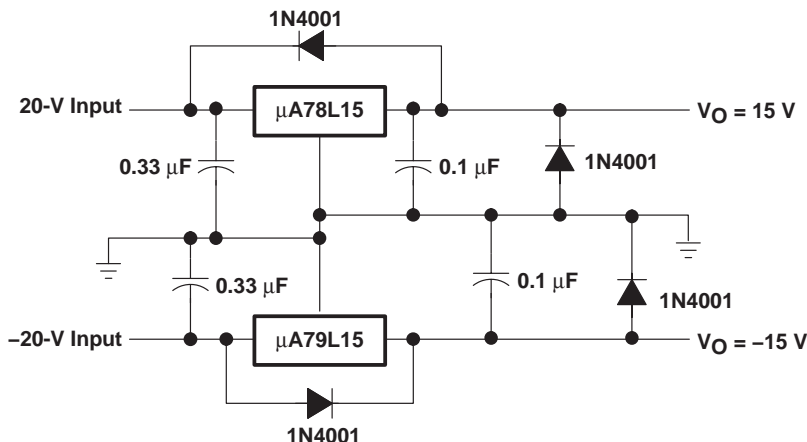


Figure 5. Regulated Dual Supply

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

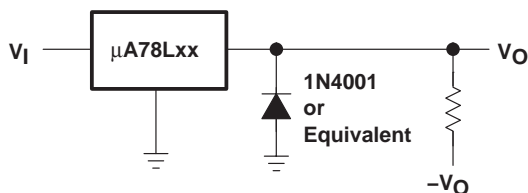


Figure 6. Output Polarity-Reversal-Protection Circuit

reverse-bias protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 7.

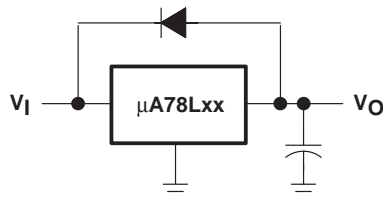


Figure 7. Reverse-Bias-Protection Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UA78L02ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L02ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L02ACDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L02ACLPL	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L02CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L02CLPL	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L05ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05ACLPL	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05ACLPLM	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05ACLPLR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L05ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
UA78L05AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05AILPL	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05AILPLR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05AIPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L05AQD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L05AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UA78L05CLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05CLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L05QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L05QLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L06ACD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L06ACDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L06ACLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L06ACLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L06ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L06CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L08ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08ACLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L08ACLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L08ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L08AILP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L08AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L08CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L08CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L08CPK	OBSOLETE	SOT-89	PK	3		TBD	Call TI	Call TI
UA78L09ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L09ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L09ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L09ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L09ACLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L09ACLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L09ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UA78L09AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L09CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L09CLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L10ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L10ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L10ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L10ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L10ACLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L10ACLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L10ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L10CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L10CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L10CLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L12ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L12ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L12ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L12ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L12ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L12ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L12ACLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
UA78L12ACLPM	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L12ACLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L12ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L12ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
UA78L12AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L12AQLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L12CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L12CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
UA78L15ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L15ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L15ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L15ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA78L15ACLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UA78L15ACLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
UA78L15ACPK	ACTIVE	SOT-89	PK	3	1000	TBD	CU SNPB	Level-1-220C-UNLIM
UA78L15ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
UA78L15CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA78L15CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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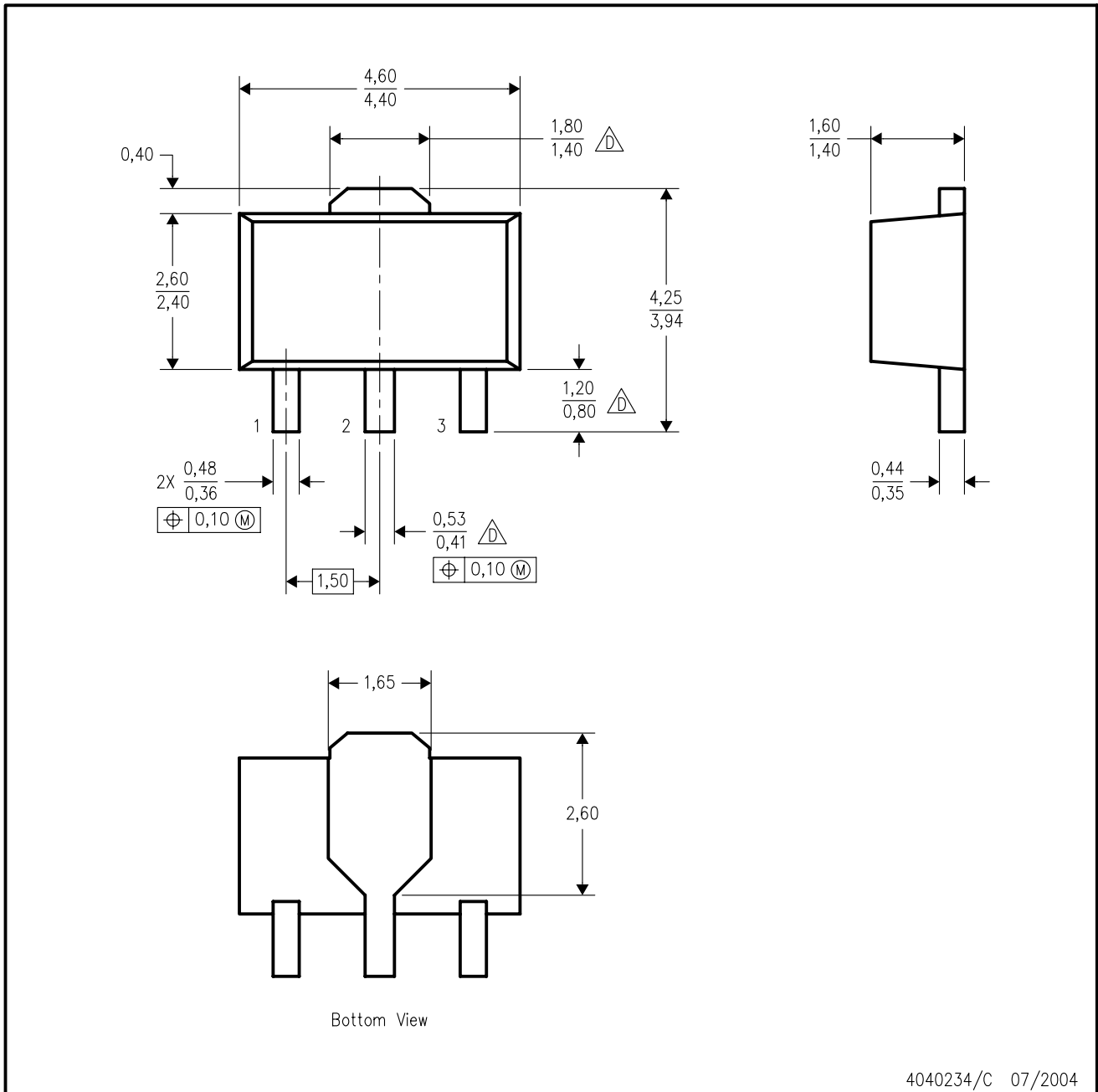
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.


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PK (R-PSSO-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. The center lead is in electrical contact with the tab.
-  Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, and minimum tab width.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Lead dimensions are not controlled within this area
 D. Falls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)
 E. Shipping Method:
 Straight lead option available in bulk pack only.
 Formed lead option available in tape & reel or ammo pack.

MECHANICAL DATA

MSOT002A – OCTOBER 1994 – REVISED NOVEMBER 2001

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Tape and Reel information for the Format Lead Option package.

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