



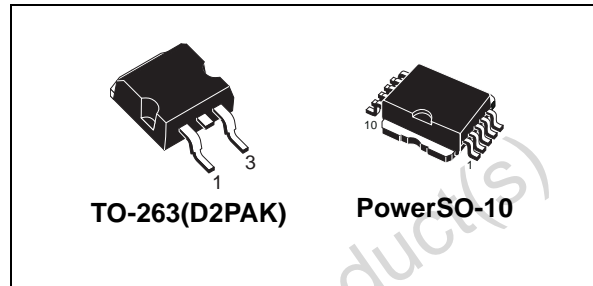
## VNB49N04 - VNV49N04

OMNIFET:  
fully autoprotected Power MOSFET

### Features

Type	V <sub>CLAMP</sub>	R <sub>DS(ON)</sub>	I <sub>LIM</sub>
VNB49N04	42 V	20 mΩ	49 A
VNV49N04			

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



### Description

The VNB49N04, VNV49N04 are monolithic devices designed in STMicroelectronics™ VIPower™ M0 technology, intended for replacement of standard Power MOSFETs from DC up to 50 KHz applications.

Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order code	
	Tube	Tape and reel
PowerSO-10	VNV49N04	VNV49N0413TR
TO-263 (D2PAK)	VNB49N04	VNB49N0413TR

# Contents

<b>1</b>	<b>Block diagram</b> .....	<b>5</b>
<b>2</b>	<b>Electrical specifications</b> .....	<b>6</b>
2.1	Absolute maximum rating .....	6
2.2	Thermal data .....	6
2.3	Electrical characteristics .....	7
2.4	Electrical characteristics curves .....	9
2.5	Waveforms .....	13
<b>3</b>	<b>Protection features</b> .....	<b>16</b>
<b>4</b>	<b>Package and packing information</b> .....	<b>17</b>
4.1	ECOPACK® .....	17
4.2	TO-263 (D2PAK) mechanical data .....	17
4.3	PowerSO-10 mechanical data .....	19
<b>5</b>	<b>Revision history</b> .....	<b>21</b>

Obsolete Product(s) - Obsolete Product(s)

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Absolute maximum rating . . . . .	6
Table 3.	Thermal data . . . . .	6
Table 4.	Off . . . . .	7
Table 5.	On . . . . .	7
Table 6.	Dynamic . . . . .	7
Table 7.	Switching . . . . .	7
Table 8.	Source drain diode . . . . .	8
Table 9.	Protections . . . . .	8
Table 10.	TO-263 (D2PAK) mechanical data . . . . .	17
Table 11.	PowerSO-10 mechanical data . . . . .	19
Table 12.	Document revision history . . . . .	21

Obsolete Product(s) - Obsolete Product(s)

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Connection diagram (top view) . . . . .	5
Figure 3.	Thermal impedance for D2PAK / PowerSO-10 . . . . .	9
Figure 4.	Derating curve . . . . .	9
Figure 5.	Output characteristics . . . . .	9
Figure 6.	Transconductance . . . . .	9
Figure 7.	Static drain-source on resistance vs input voltage . . . . .	9
Figure 8.	Static drain-source on resistance (part 1) . . . . .	9
Figure 9.	Static drain-source on resistance (part 2) . . . . .	10
Figure 10.	Input charge vs input voltage . . . . .	10
Figure 11.	Capacitance variations . . . . .	10
Figure 12.	Normalized input threshold voltage vs temperature . . . . .	10
Figure 13.	Normalized on resistance vs temperature (part 1) . . . . .	10
Figure 14.	Normalized on resistance vs temperature (part 2) . . . . .	10
Figure 15.	Turn-on current slope (part 1) . . . . .	11
Figure 16.	Turn-on current slope (part 2) . . . . .	11
Figure 17.	Turn-off drain-source voltage slope (part 1) . . . . .	11
Figure 18.	Turn-off drain-source voltage slope (part 2) . . . . .	11
Figure 19.	Switching time resistive load vs $R_G$ (part 1) . . . . .	11
Figure 20.	Switching time resistive load vs $R_G$ (part 2) . . . . .	11
Figure 21.	Switching time resistive load vs $V_{IN}$ . . . . .	12
Figure 22.	Current limit vs junction temperature . . . . .	12
Figure 23.	Step response current limit . . . . .	12
Figure 24.	Source drain diode forward characteristics . . . . .	12
Figure 25.	Unclamped inductive load test circuits . . . . .	13
Figure 26.	Unclamped inductive waveforms . . . . .	13
Figure 27.	Switching time test circuits for resistive load . . . . .	14
Figure 28.	Input charge test circuit . . . . .	14
Figure 29.	Test circuit for inductive load switching and diode recovery times . . . . .	15
Figure 30.	Waveforms . . . . .	15
Figure 31.	TO-263 (D2PAK) package dimension . . . . .	18
Figure 32.	PowerSO-10 package dimension . . . . .	20

# 1 Block diagram

Figure 1. Block diagram

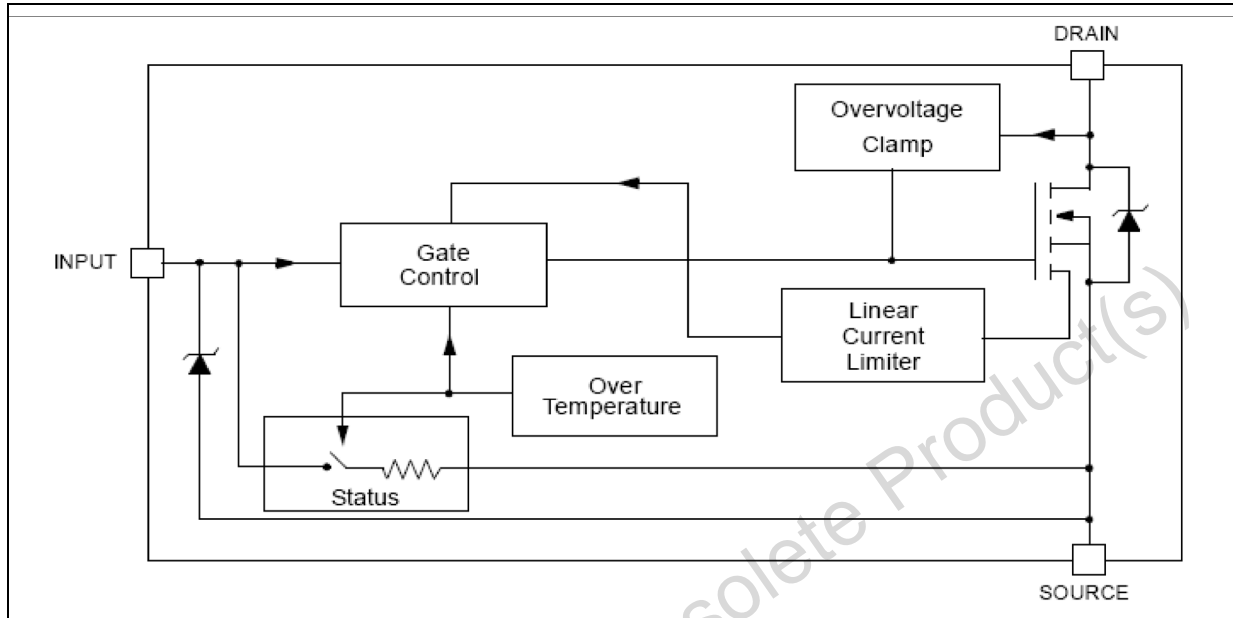
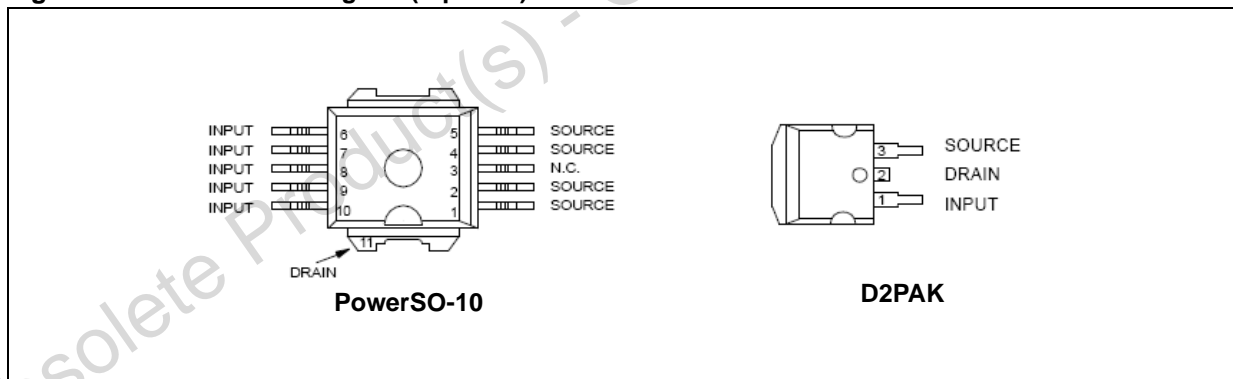


Figure 2. Connection diagram (top view)



## 2 Electrical specifications

### 2.1 Absolute maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 2. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{IN} = 0\text{ V}$ )	Internally clamped	V
$V_{IN}$	Input voltage	18	V
$I_D$	Drain current	Internally limited	A
$I_R$	Reverse DC output current	-50	A
$V_{ESD}$	Electrostatic discharge ( $R = 1.5\text{ K}\Omega$ , $C = 100\text{ pF}$ )	2000	V
$P_{tot}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
$T_j$	Operating junction temperature	Internally limited	$^\circ\text{C}$
$T_C$	Case operating temperature	Internally limited	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

### 2.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		PowerSO-10	D2PAK	
$R_{thj-case}$	Thermal resistance junction-case (max)	1	1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (max)	50	62.5	$^\circ\text{C}/\text{W}$

## 2.3 Electrical characteristics

-40 °C < T<sub>j</sub> < 125 °C, unless otherwise specified

**Table 4. Off**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>CLAMP</sub>	Drain-source clamp voltage	I <sub>D</sub> = 200 mA; V <sub>IN</sub> = 0	34	42	50	V
V <sub>CLTH</sub>	Drain-source clamp threshold voltage	I <sub>D</sub> = 2 mA; V <sub>IN</sub> = 0	33			V
V <sub>INCL</sub>	Input-source reverse clamp voltage	I <sub>IN</sub> = -1 mA	-1.2		-0.1	V
I <sub>DSS</sub>	Zero input voltage drain current (V <sub>IN</sub> = 0 V)	V <sub>DS</sub> = 13 V; V <sub>IN</sub> = 0 V			70	μA
		V <sub>DS</sub> = 25 V; V <sub>IN</sub> = 0 V			220	μA
I <sub>ISS</sub>	Supply current from input pin	V <sub>DS</sub> = 0 V; V <sub>IN</sub> = 10 V		250	550	μA

**Table 5. On<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>IN(th)</sub>	Input threshold voltage	V <sub>DS</sub> = V <sub>IN</sub> ; I <sub>D</sub> + I <sub>IN</sub> = 1 mA	0.8	—	3	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>IN</sub> = 10 V; I <sub>D</sub> = 25 A		—	0.04	Ω
		V <sub>IN</sub> = 5 V; I <sub>D</sub> = 25 A		—	0.05	Ω

1. Pulsed; pulse duration = 300μs, duty cycle 1.5%

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 13 V; I <sub>D</sub> = 25 A; T <sub>c</sub> = 25 °C	25	30		S
C <sub>OSS</sub>	Output capacitance	V <sub>DS</sub> = 13 V; f = 1 MHz; V <sub>IN</sub> = 0 V; T <sub>c</sub> = 25 °C		1100	1500	pF

1. Pulsed; pulse duration = 300μs, duty cycle 1.5%

**Table 7. Switching<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 25 A; V <sub>gen</sub> = 10 V; R <sub>gen</sub> = 10 Ω; (see <a href="#">Figure 27</a> )	—	200	600	ns
t <sub>r</sub>	Rise time		—	1300	3600	ns
t <sub>d(off)</sub>	Turn-off delay time		—	800	2400	ns
t <sub>f</sub>	Fall time		—	300	900	ns

Table 7. Switching<sup>(1)</sup> (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 15\text{ V}; I_D = 25\text{ A}; V_{gen} = 10\text{ V};$ $R_{gen} = 1000\ \Omega$ (see <a href="#">Figure 27</a> )	—	1.3	3.8	$\mu\text{s}$
$t_r$	Rise time		—	3.8	10.4	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time		—	12	24	$\mu\text{s}$
$t_f$	Fall time		—	6.1	17	$\mu\text{s}$
$(di/dt)_{on}$	Turn-on current slope	$V_{DS} = 15\text{ V}; I_D = 25\text{ A}; V_{IN} = 10\text{ V};$ $R_{gen} = 10\ \Omega$	—	25		$\text{A}/\mu\text{s}$
$Q_i$	Total input charge	$V_{DS} = 15\text{ V}; I_D = 25\text{ A}; V_{IN} = 10\text{ V}$	—	100		nC

1. Parameters guaranteed by design/characterization

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 25\text{ A}; V_{IN} = 0\text{ V}$	—		1.8	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 25\text{ A}; di/dt = 100\text{ A}/\mu\text{s};$ $V_{DS} = 30\text{ V}; T_j = 25\text{ }^\circ\text{C};$ (see <a href="#">Figure 29</a> )	—	250		ns
$Q_{rr}^{(2)}$	Reverse recovery charge		—	910		nC
$I_{RRM}^{(2)}$	Reverse recovery current		—	7.5		A

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

2. Parameters guaranteed by design/characterization.

Table 9. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ILIM	Drain current limit	$V_{IN} = 10\text{ V}; V_{DS} = 13\text{ V}$	28	49	70	A
		$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$	28	49	70	A
$t_{dlim}^{(1)}$	Step response current limit	$V_{IN} = 10\text{ V}$		35	50	$\mu\text{s}$
		$V_{IN} = 5\text{ V}$		90	150	$\mu\text{s}$
$T_{jsh}^{(1)}$	Overtemperature shutdown		150			$^\circ\text{C}$
$T_{jrs}^{(1)}$	Overtemperature reset		135			$^\circ\text{C}$
$I_{gf}^{(1)}$	Fault sink current	$V_{IN} = 10\text{ V}; V_{DS} = 13\text{ V}$		50		mA
		$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$		20		mA
$E_{as}^{(1)}$	Single pulse avalanche energy	Starting $T_j = 25\text{ }^\circ\text{C}; V_{DS} = 20\text{ V};$ $V_{IN} = 10\text{ V}; R_{gen} = 1\text{ K}\Omega; L = 6\text{ mH}$	4			J

1. Parameters guaranteed by design/characterization.



## 2.4 Electrical characteristics curves

Figure 3. Thermal impedance for D2PAK / PowerSO-10

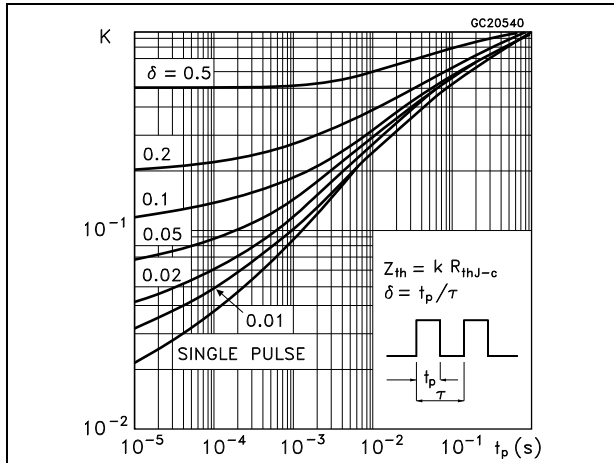


Figure 4. Derating curve

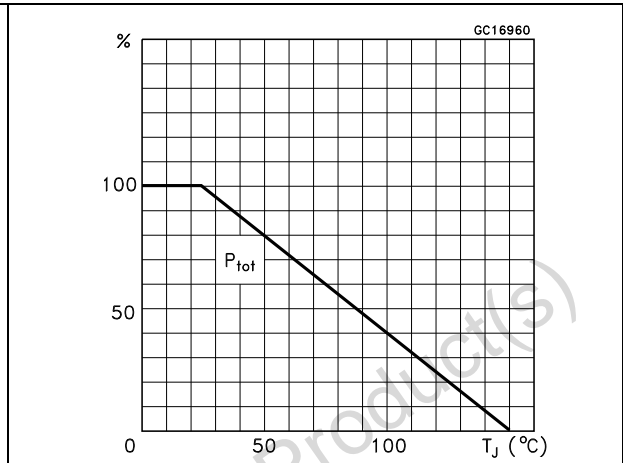


Figure 5. Output characteristics

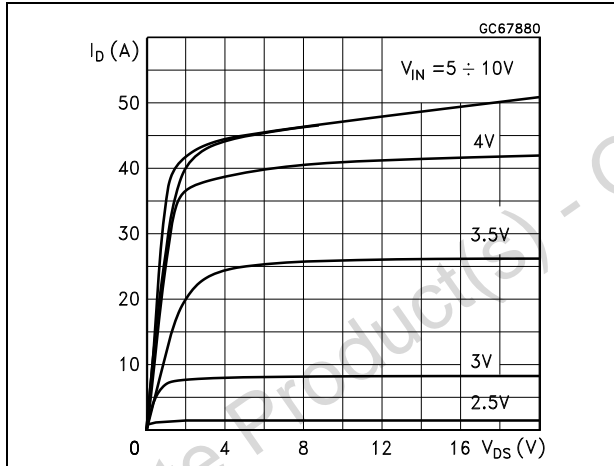


Figure 6. Transconductance

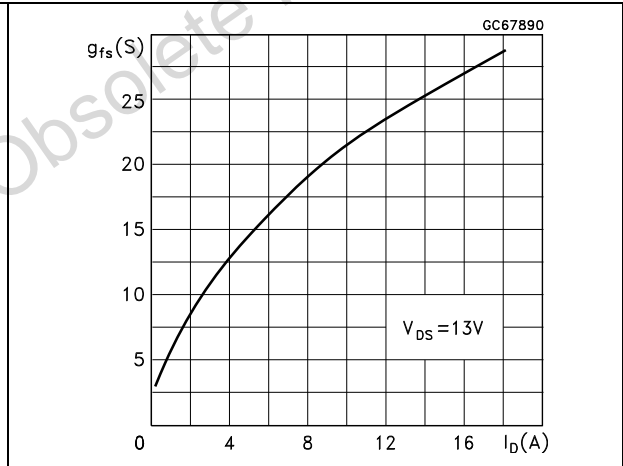


Figure 7. Static drain-source on resistance vs input voltage

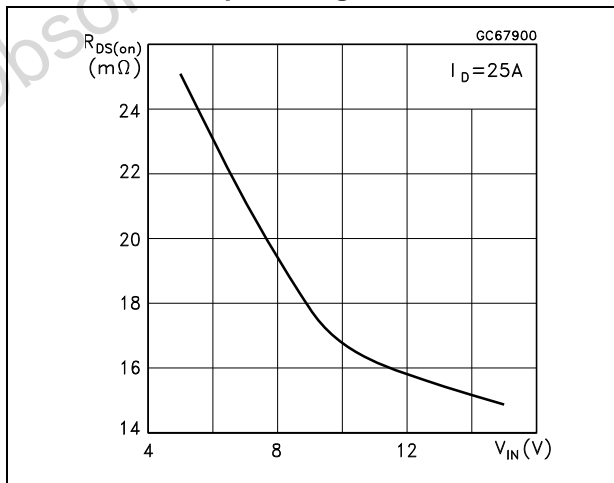


Figure 8. Static drain-source on resistance (part 1)

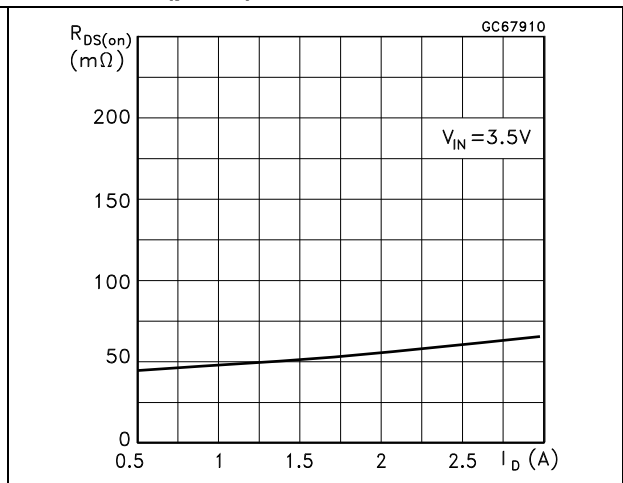


Figure 9. Static drain-source on resistance (part 2)

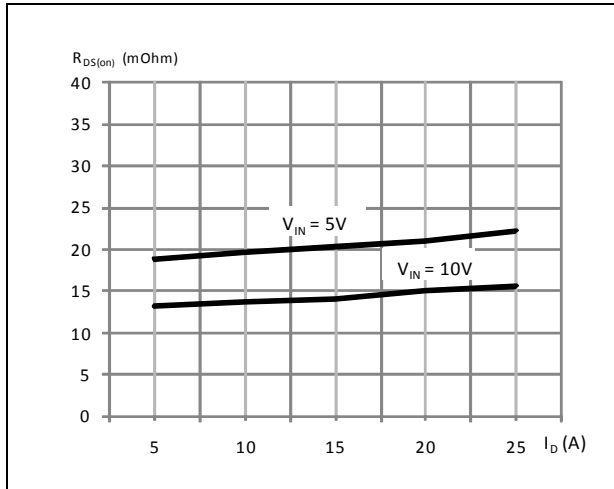


Figure 10. Input charge vs input voltage

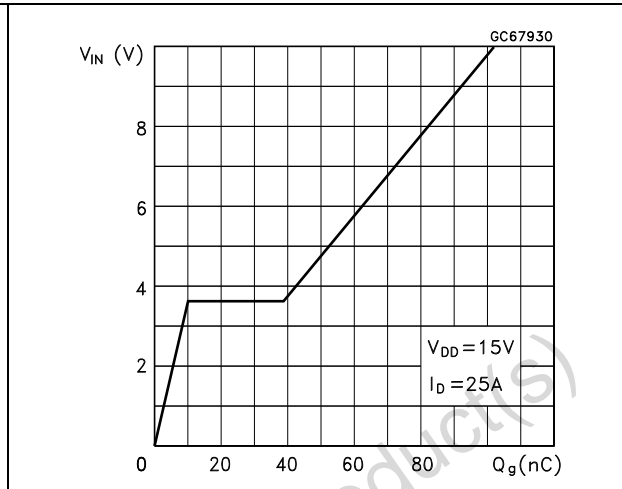


Figure 11. Capacitance variations

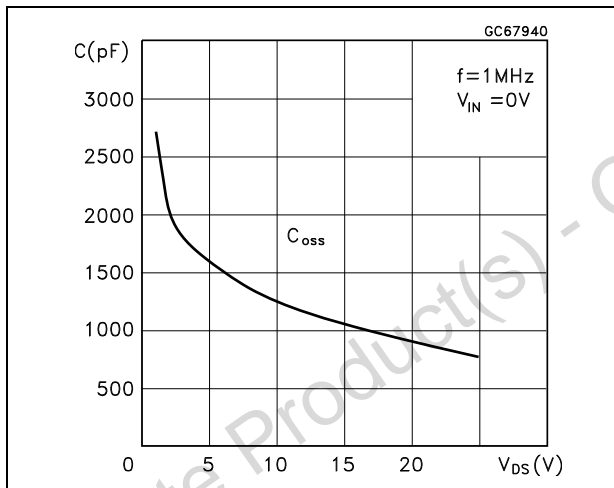


Figure 12. Normalized input threshold voltage vs temperature

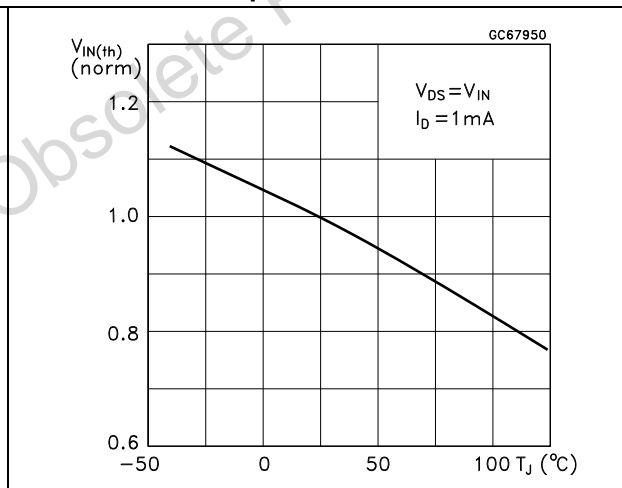


Figure 13. Normalized on resistance vs temperature (part 1)

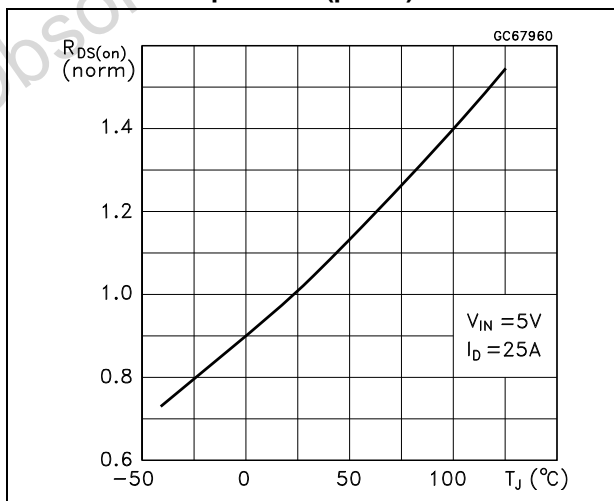


Figure 14. Normalized on resistance vs temperature (part 2)

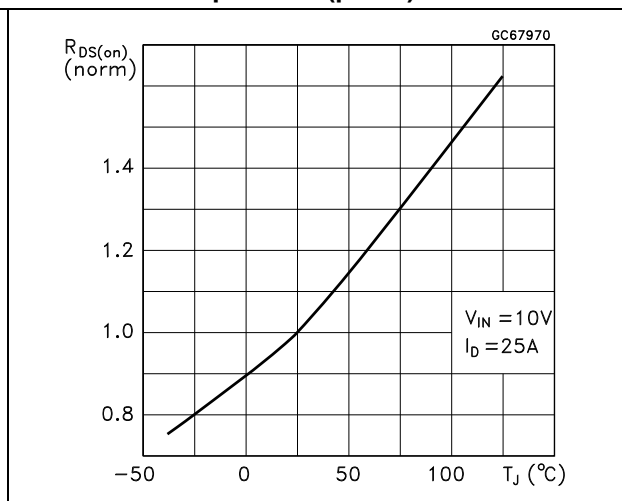


Figure 15. Turn-on current slope (part 1)

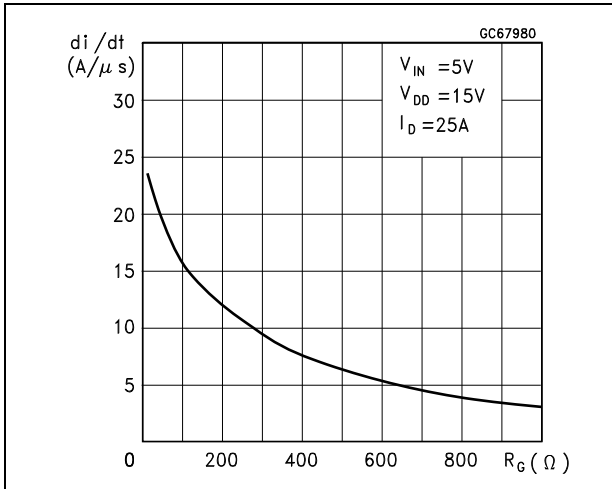


Figure 16. Turn-on current slope (part 2)

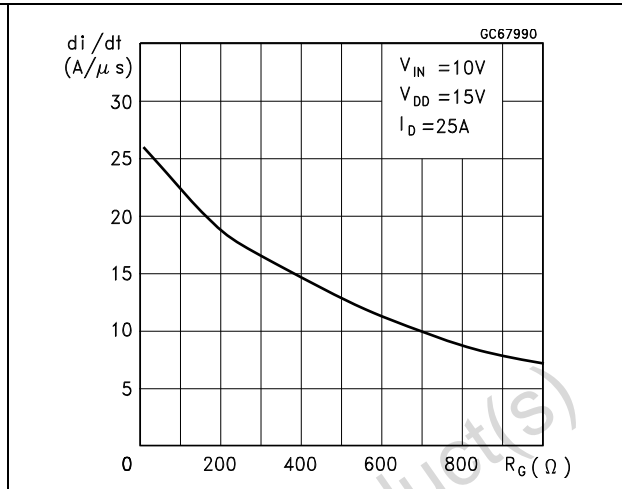


Figure 17. Turn-off drain-source voltage slope (part 1)

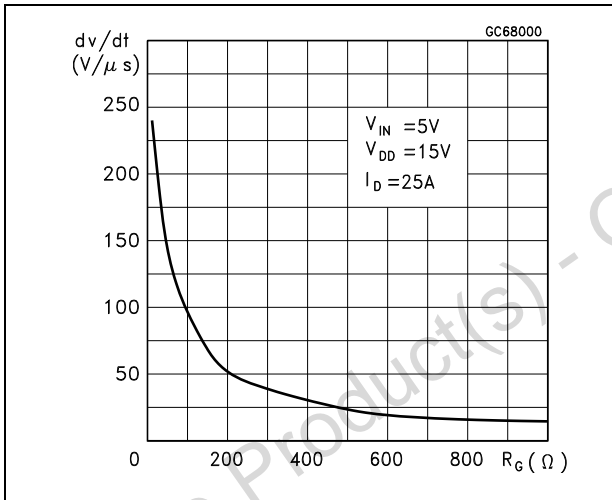


Figure 18. Turn-off drain-source voltage slope (part 2)

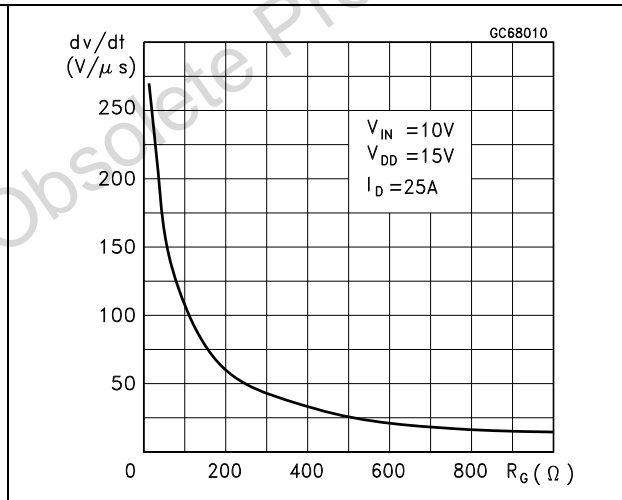


Figure 19. Switching time resistive load vs Rg (part 1)

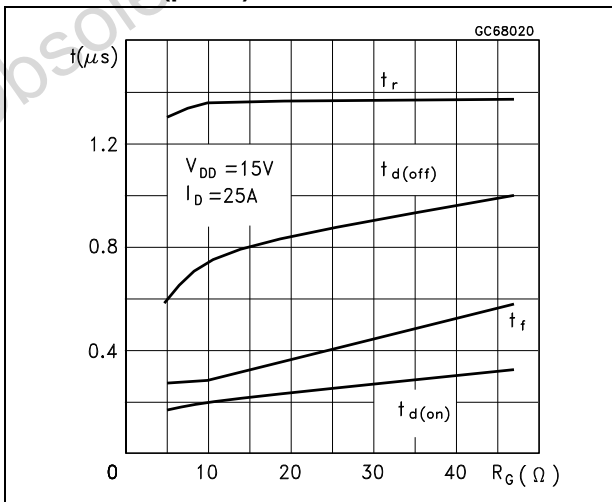


Figure 20. Switching time resistive load vs Rg (part 2)

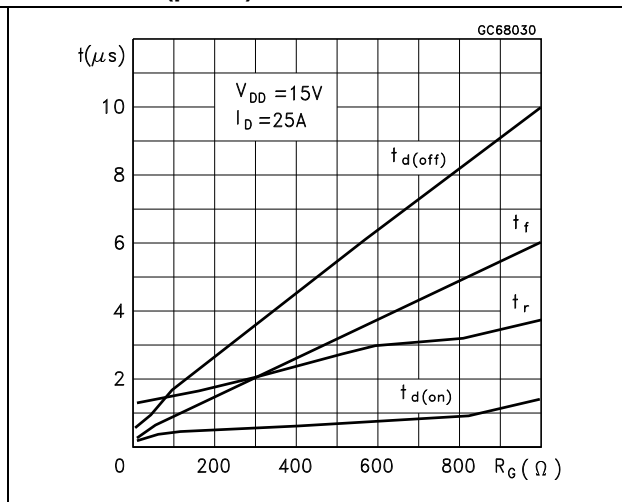


Figure 21. Switching time resistive load vs  $V_{IN}$  Figure 22. Current limit vs junction temperature

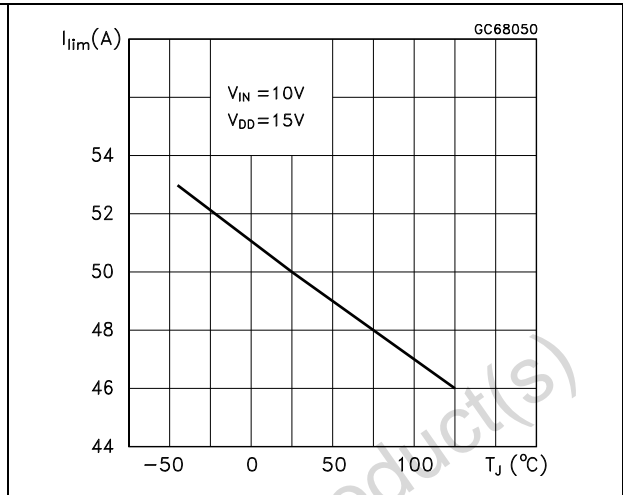
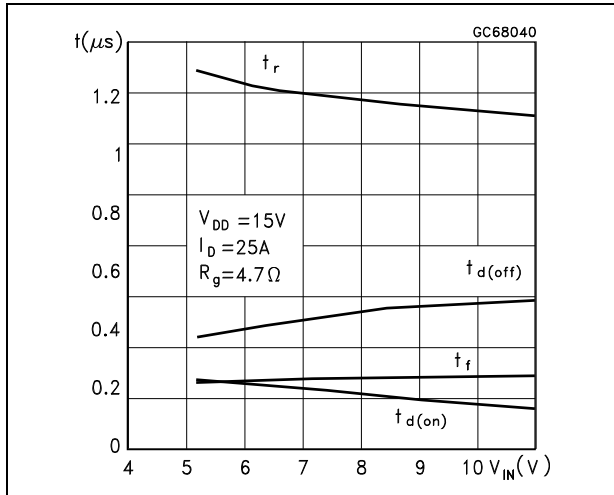
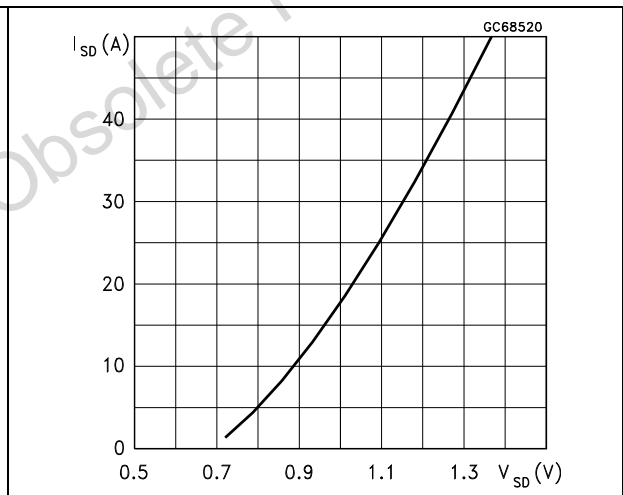
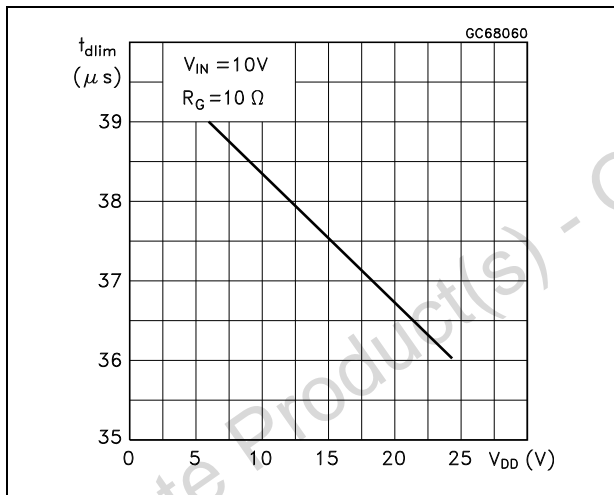


Figure 23. Step response current limit

Figure 24. Source drain diode forward characteristics



## 2.5 Waveforms

Figure 25. Unclamped inductive load test circuits

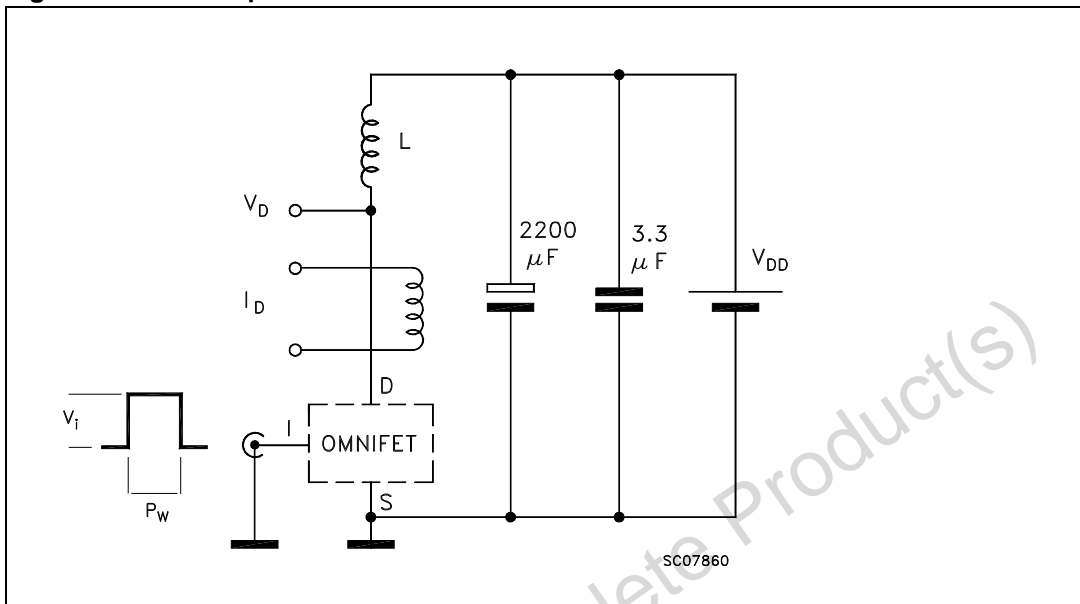


Figure 26. Unclamped inductive waveforms

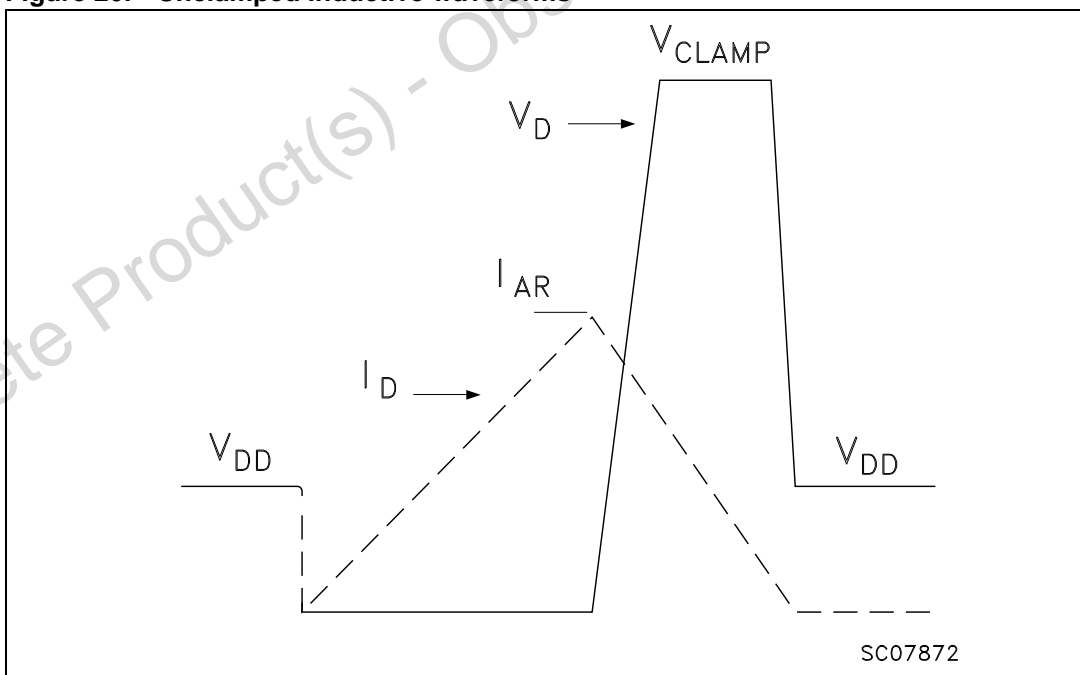


Figure 27. Switching time test circuits for resistive load

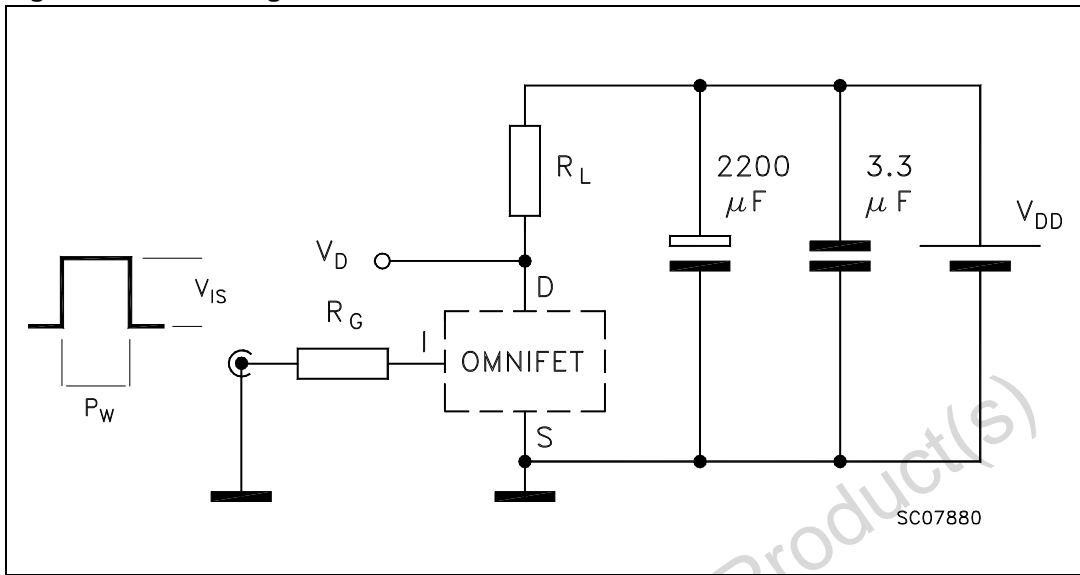


Figure 28. Input charge test circuit

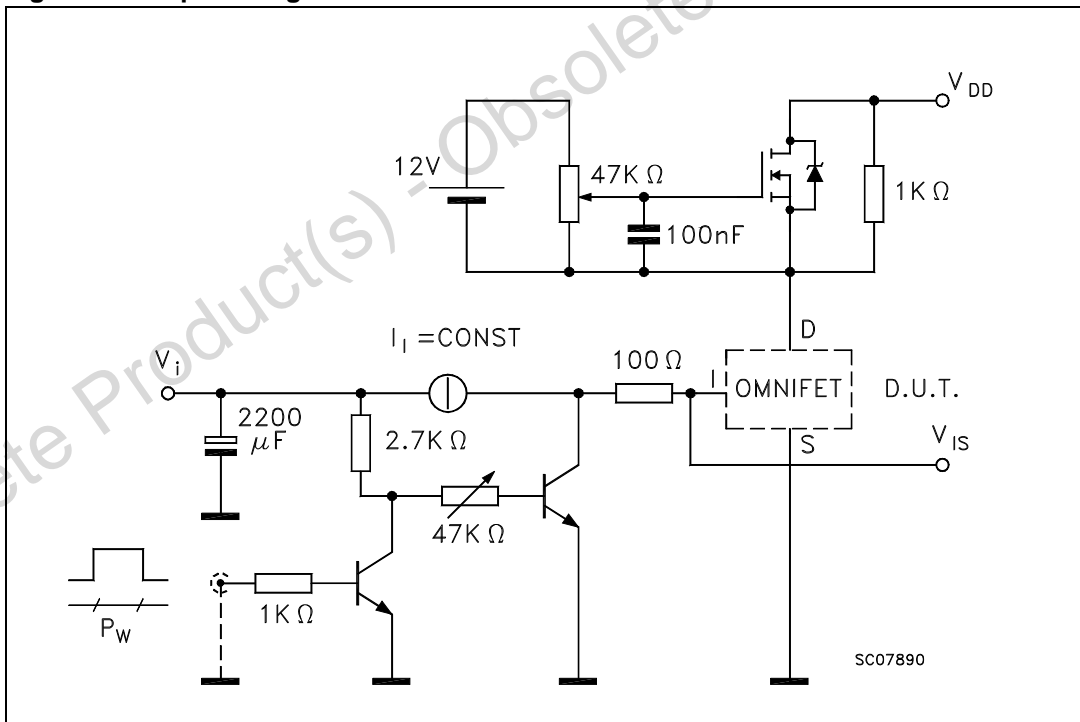


Figure 29. Test circuit for inductive load switching and diode recovery times

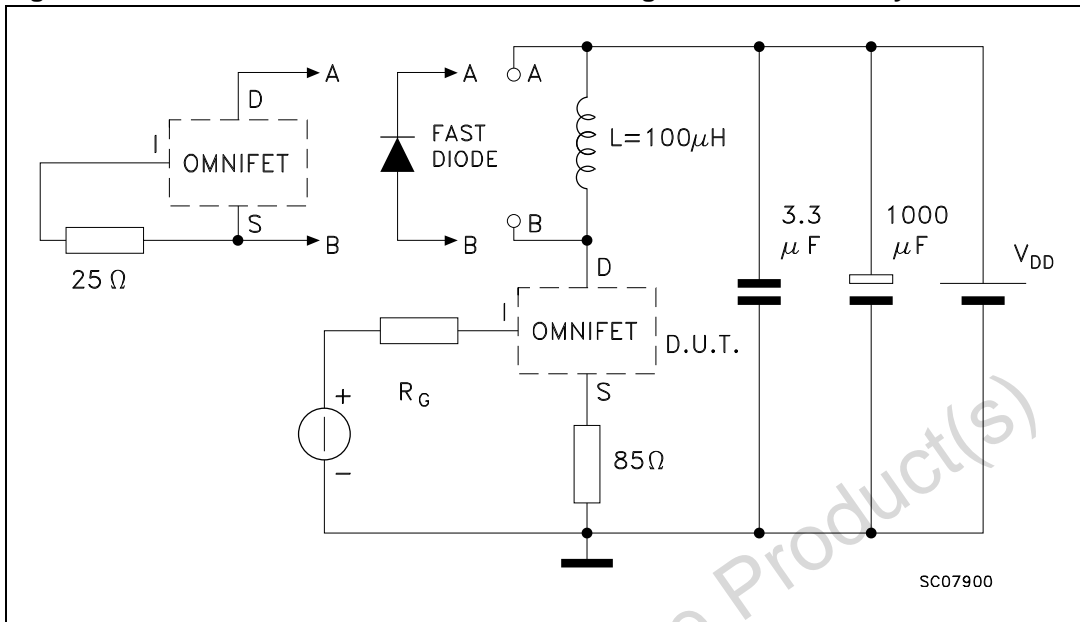
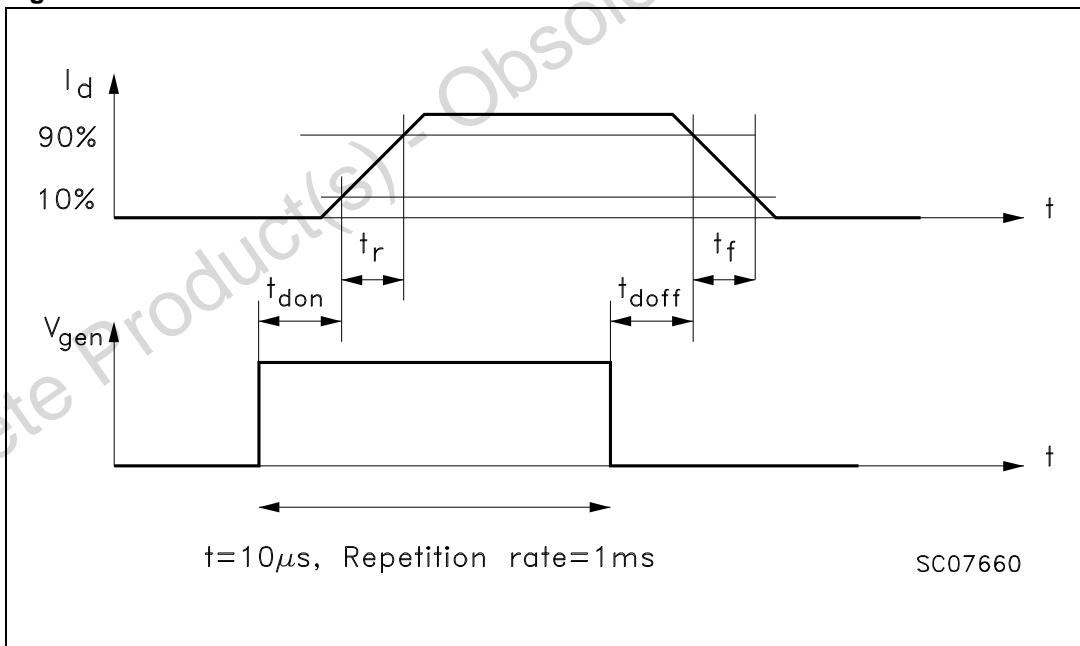


Figure 30. Waveforms



### 3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50 KHz. The only difference

from the user's standpoint is that a small DC current (I<sub>ISS</sub>) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- **Overvoltage clamp protection:**  
Internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **Linear current limiter circuit:**  
Limits the drain current I<sub>D</sub> to I<sub>LIM</sub> whatever the INPUT pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T<sub>jsh</sub>.
- **Overtemperature and short circuit protection:**  
These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150 °C. The device is automatically restarted when the chip temperature falls below 135 °C.
- **Status feedback:**  
In the case of an overtemperature fault condition, a status feedback is provided through the INPUT pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100Ω. The failure can be detected by monitoring the voltage at the INPUT pin, which will be close to ground potential. Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in R<sub>DS(ON)</sub>).



## 4 Package and packing information

### 4.1 ECOPACK®

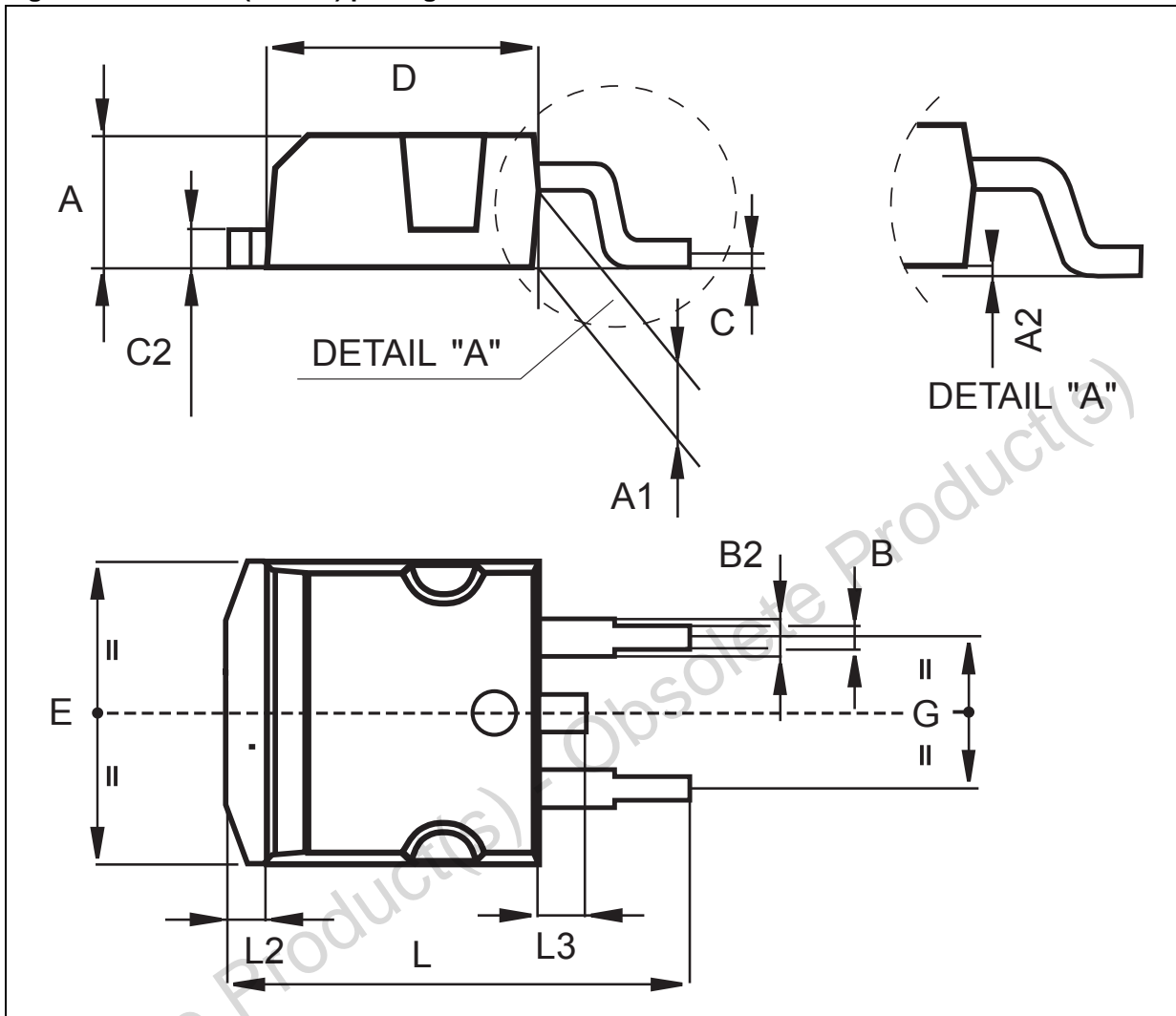
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.2 TO-263 (D2PAK) mechanical data

Table 10. TO-263 (D2PAK) mechanical data

Dim.	mm.			Inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.30	—	4.60	0.169	—	0.181
A1	2.49	—	2.69	0.098	—	0.106
B	0.70	—	0.93	0.027	—	0.036
B2	1.25	—	1.4	0.049	—	0.055
C	0.45	—	0.6	0.017	—	0.023
C2	1.21	—	1.36	0.047	—	0.053
D	8.95	—	9.35	0.352	—	0.368
E	10	—	10.28	0.393	—	0.404
G	4.88	—	5.28	0.192	—	0.208
L	15	—	15.85	0.590	—	0.625
L2	1.27	—	1.4	0.050	—	0.055
L3	1.4	—	1.75	0.055	—	0.068

Figure 31. TO-263 (D2PAK) package dimension

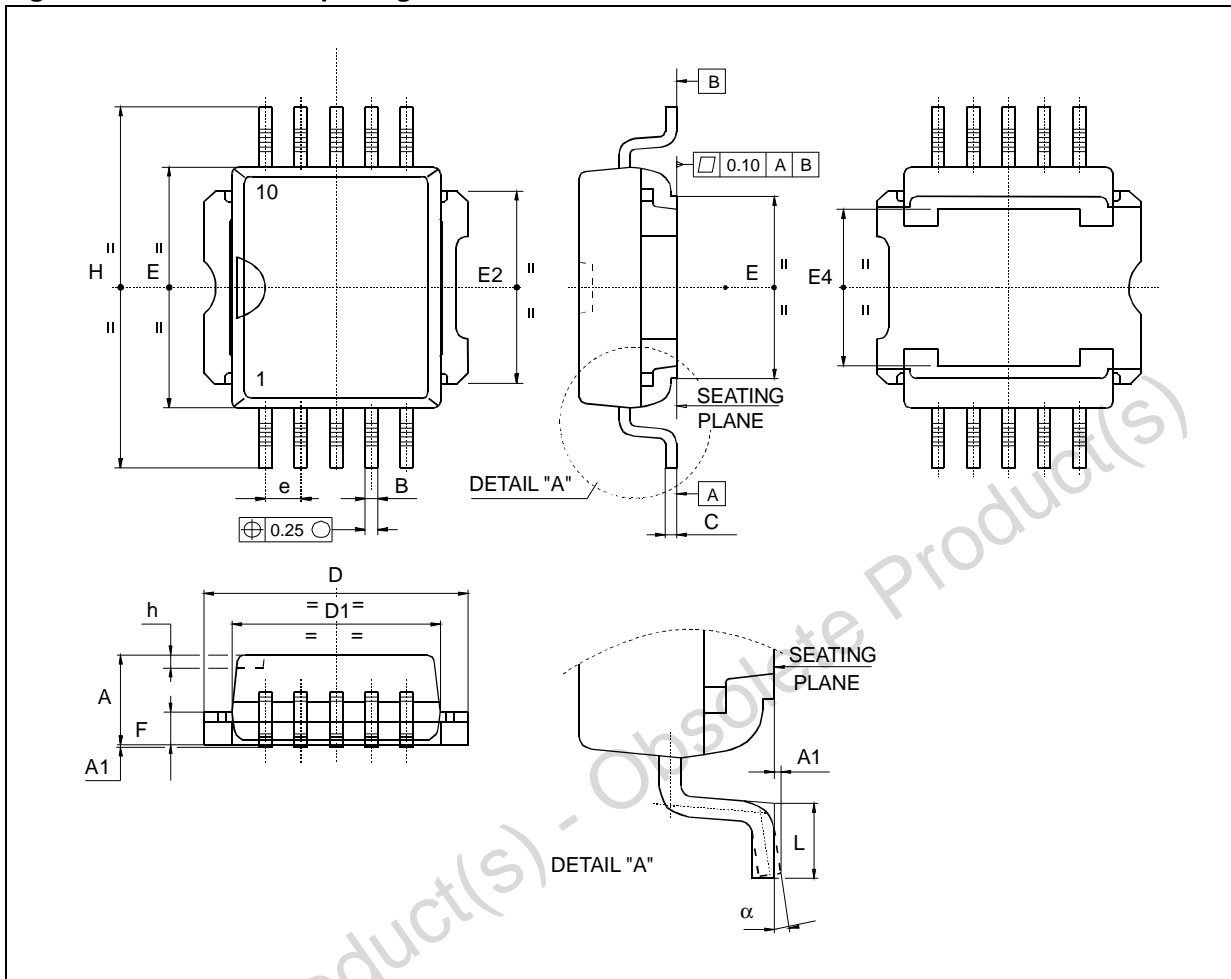


### 4.3 PowerSO-10 mechanical data

Table 11. PowerSO-10 mechanical data

Dim.	mm.			Inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
Q		1.70			0.067	
	0°		8°			

Figure 32. PowerSO-10 package dimension



## 5 Revision history

Table 12. Document revision history

Date	Revision	Change
01-Oct-1999	1	Initial release.
25-Nov-2010	2	Changed document template. Removed ISOWATT220 package. Updated <a href="#">Figure 9: Static drain-source on resistance (part 2)</a>
20-Sep-2013	3	Updated Disclaimer.

Obsolete Product(s) - Obsolete Product(s)

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)